ATtiny416/816

AVR® Microcontroller with Core Independent Peripherals and picoPower® Technology

Introduction

The ATtiny416/816 microcontrollers are using the high-performance low-power AVR® RISC architecture, and is capable of running at up to 20MHz, with up to 4/8KB Flash, 256/512bytes of SRAM and 128bytes of EEPROM in a 20-pin package. The series uses the latest technologies with a flexible and low power architecture including Event System and SleepWalking, accurate analog features and advanced peripherals. Capacitive touch interfaces with driven shield are supported with the integrated QTouch® peripheral touch controller.

Features

- CPU
  - AVR® 8-bit CPU
  - Running at up to 20MHz
  - Single Cycle I/O Access
  - Two-level Interrupt Controller
  - Two-cycle Hardware Multiplier
- Memories
  - 4/8KB In-system self-programmable Flash Memory
  - 128B EEPROM
  - 256/512B SRAM
- System
  - Power-on Reset (POR)
  - Brown-out Detection (BOD)
  - Clock Options:
    - 16/20MHz Low Power Internal RC Oscillator
    - 32.768kHz Ultra Low Power (ULP) Internal RC Oscillator
    - 32.768kHz External Crystal Oscillator
    - External Clock Input
  - Single Pin Unified Program Debug Interface (UPDI)
  - Three Sleep Modes:
    - Idle with All Peripherals Running and Mode for Immediate Wake Up Time
    - Standby
      - Configurable Operation of Selected Peripherals
      - SleepWalking Peripherals
    - Power Down with Wake-up Functionality

- Peripherals
  - 6-channel Event System
  - One 16-bit Timer/Counter Type A with Dedicated Period Register, Three Compare Channels (TCA)
  - One 16-bit Timer/Counter type B with Input Capture (TCB)
  - One 12-bit Timer/Counter type D Optimized for Control Applications (TCD)
  - One 16-bit Real Time Counter (RTC) Running from External Crystal or Internal RC Oscillator
  - One USART with Fractional Baud Rate Generator, Auto-baud, and Start-of-frame Detection
  - Master/Slave Serial Peripheral Interface (SPI)
  - Master/Slave TWI with Dual Address Match
    - Standard Mode (Sm, 100kHz)
    - Fast Mode (Fm, 400kHz)
    - Fast Mode Plus (Fm+, 1MHz)
  - Configurable Custom Logic (CCL) with Two Programmable Lookup Tables (LUT)
  - Analog Comparator (AC) with Low Propagation Delay
  - 10-bit 115ksps Analog to Digital Converter (ADC)
  - 8-bit Digital to Analog Converter (DAC)
  - Five Selectable Internal Voltage References: 0.55V, 1.1V, 1.5V, 2.5V and 4.3V
  - Automated CRC Memory Scan
  - Watchdog Timer (WDT) with Window Mode, with Separate On-chip Oscillator
  - Peripheral Touch Controller (PTC)[(1)]
    - Capacitive Touch Buttons, Sliders and Wheels
    - Wake-up on Touch
    - Driven Shield for Improved Moisture and Noise Handling Performance
    - Six Self-capacitance and Nine Mutual-capacitance Channels
  - External Interrupt on All General Purpose Pins
- I/O and Packages:
  - 18 Programmable I/O Lines
  - 20-pin VQFN 3x3 and SOIC300
- Temperature Ranges:
  - -40°C to 105°C
  - -40°C to 125°C Temperature Graded Device Options Available
- Speed Grades:
  - 0-5MHz @ 1.8V – 5.5V
  - 0-10MHz @ 2.7V – 5.5V
  - 0-20MHz @ 4.5V – 5.5V

Note:

1. Only Available in Devices with 8KB Flash.

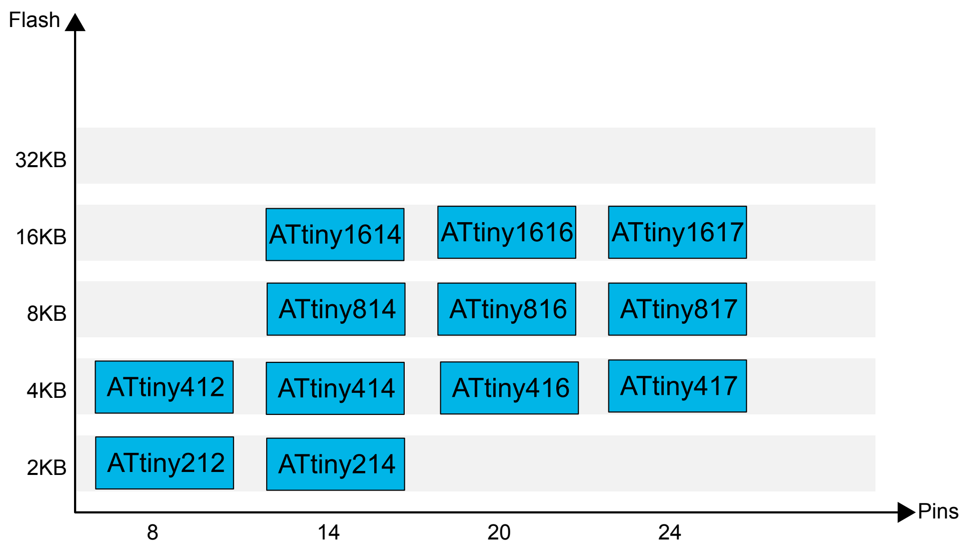
Table of Contents

1. tinyAVR® 1-Series Overview

The figure below shows the tinyAVR 1-series, laying out pin count variants and memory sizes:

- Vertical migration can be done upwards without code modification, since these devices are pin compatible and provide the same or even more features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore also the available features.

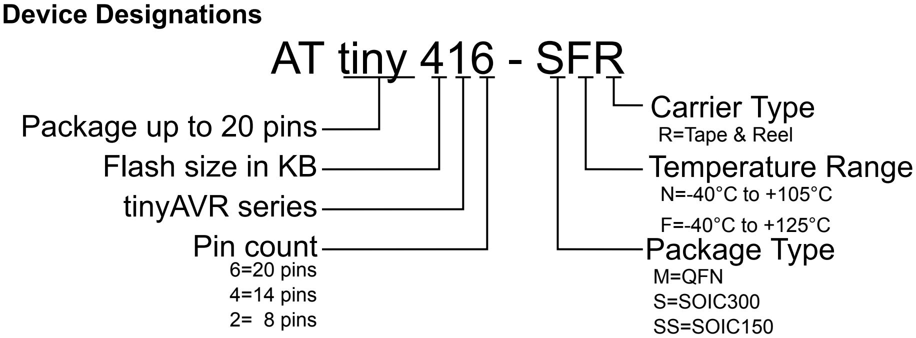
Figure 1-1. tinyAVR®1-Series Overview



Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the series contains information as depicted below:

Figure 1-2. Device Designations



1.1 Configuration Summary

1.1.1 Peripheral Summary

Table 1-1. Peripheral Summary

	ATtiny416	ATtiny816
Pins	20	20
SRAM	256B	512B
Flash	4KB	8KB
EEPROM	128B	128B
Max. frequency (MHz)	20	20
16-bit Timer/Counter type A (TCA)	1	1
16-bit Timer/Counter type B (TCB)	1	1
12-bit Timer/Counter type D (TCD)	1	1
Real Time Counter (RTC)	1	1
USART	1	1
SPI	1	1
TWI (I^2C)	1	1
ADC	1	1
ADC channels	12	12
DAC	1	1
AC	1	1
Peripheral Touch Controller (PTC)(1)	No	1
PTC number of self-capacitance channels(1)	-	6
PTC number of mutual-capacitance channels(1)	-	9
Custom Logic/Configurable Lookup Tables	1	1
Window Watchdog	1	1
Event System channels	6	6
General purpose I/O	18	18
External interrupts	18	18
CRCSCAN	1	1

Note:

1. The PTC takes control over the ADC while the PTC is used.

2. Ordering Information

2.1 ATtiny416

Table 2-1. ATtiny416 Ordering Codes

Ordering Code[(1)]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny416-MNR	4KB	VQFN 3x3 (ZCL)	20	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny416-MFR	4KB	VQFN 3x3 (ZCL)	20	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel
ATtiny416-SNR	4KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny416-SFR	4KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

2.2 ATtiny816

Table 2-2. ATtiny816 Ordering Codes

Ordering Code[(1)]	Flash	Package Type (GPC)	Leads	Power Supply	Operational Range	Carrier Type
ATtiny816-MNR	8KB	VQFN 3x3 (ZCL)	20	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny816-MFR	8KB	VQFN 3x3 (ZCL)	20	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel
ATtiny816-SNR	8KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C +105°C)	Tape & Reel
ATtiny816-SFR	8KB	SOIC300 (SRJ)	20	1.8V - 5.5V	Industrial (-40°C +125°C)	Tape & Reel

Note:

1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. Block Diagram

Figure 3-1. ATtiny416 Block Diagram

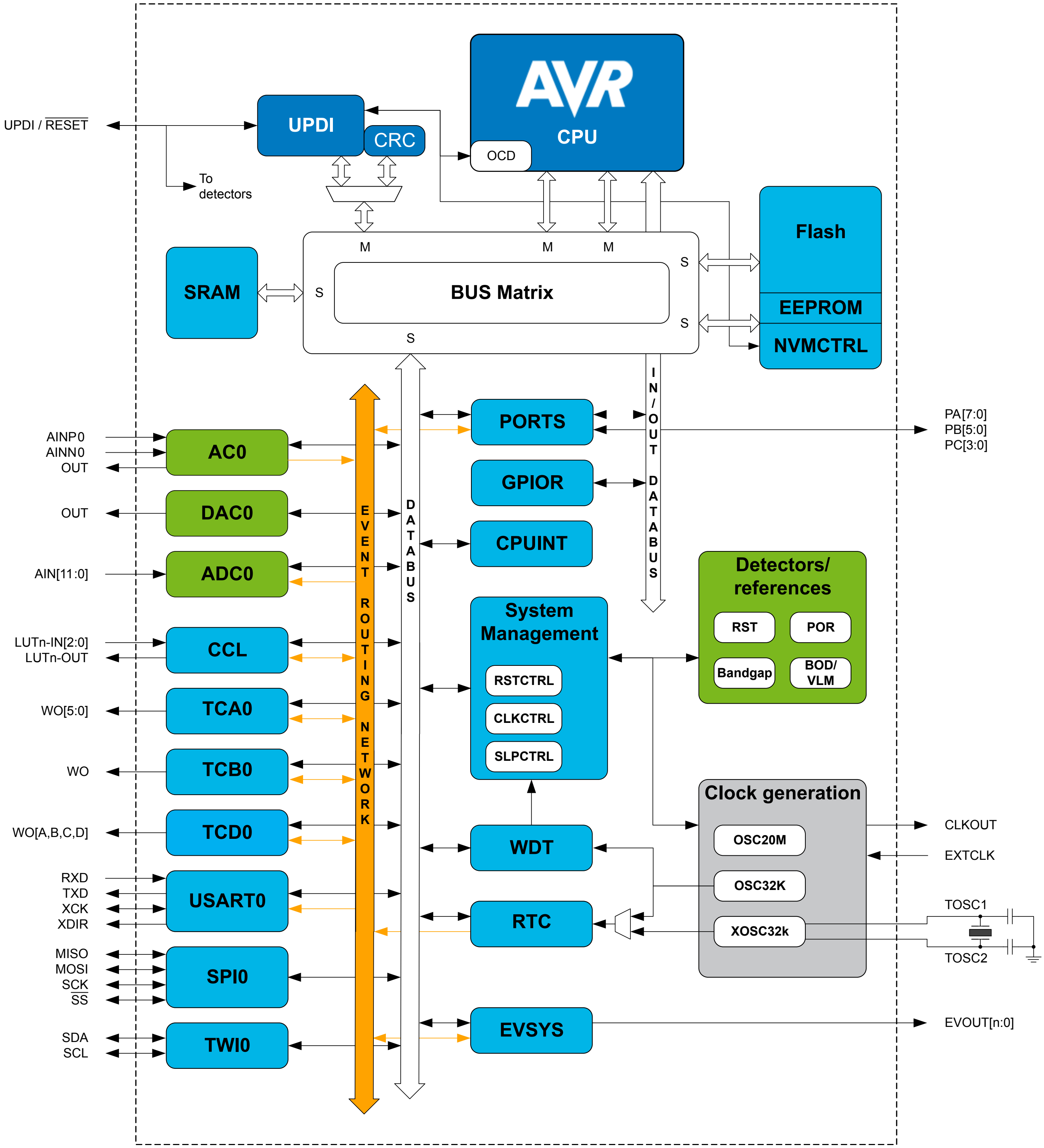
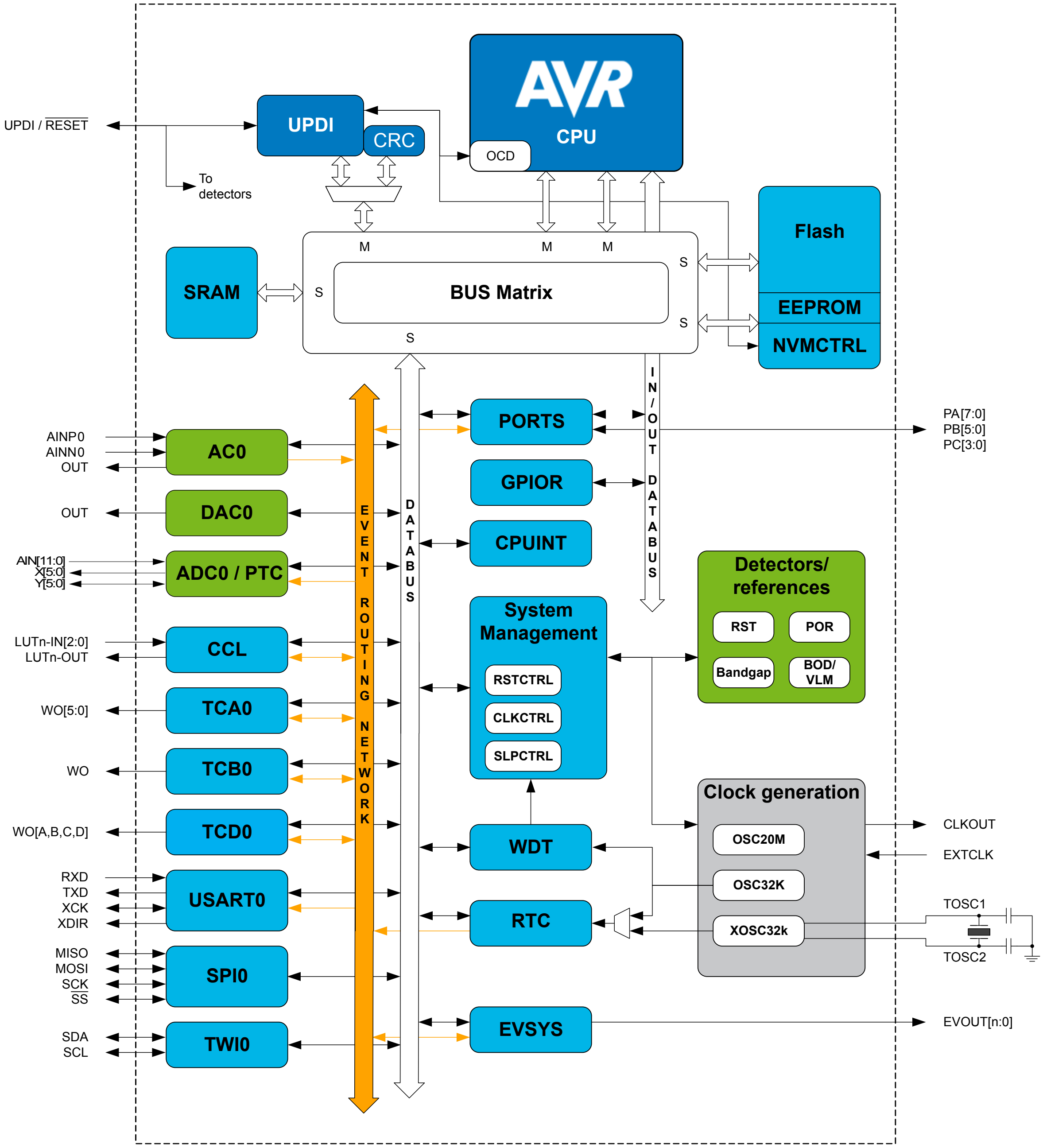
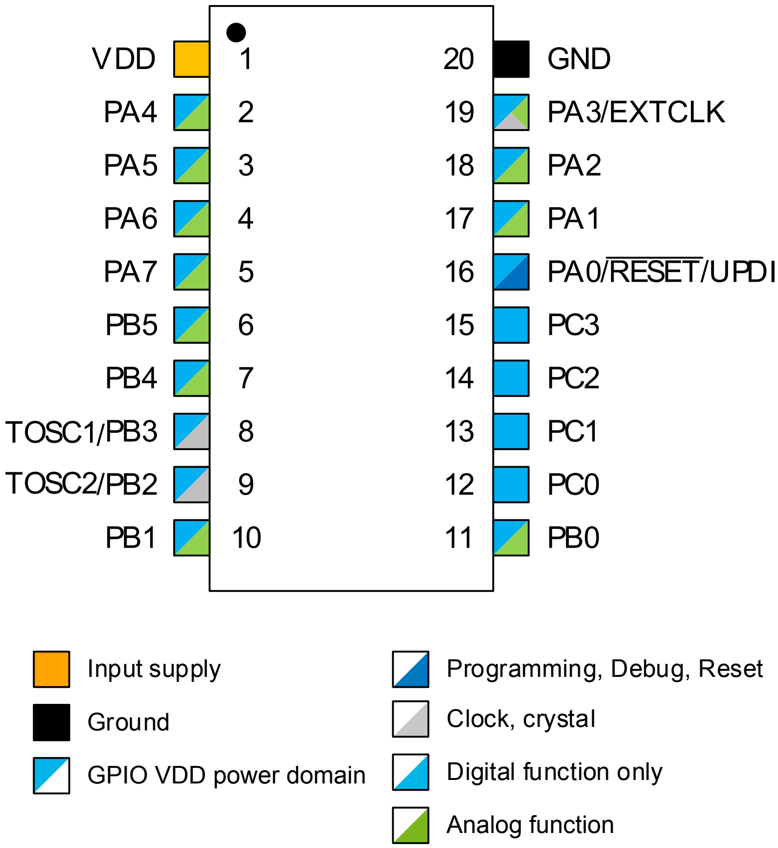


Figure 3-2. ATtiny816 Block Diagram

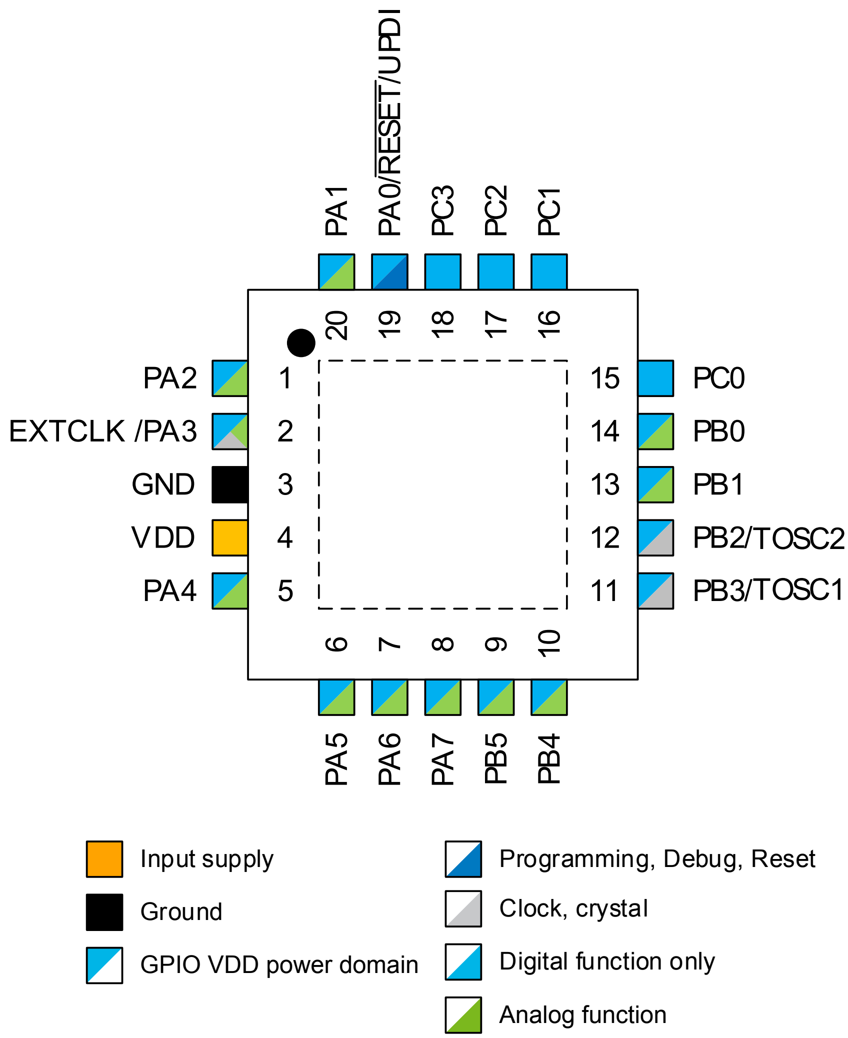


4. Pinout

4.1 20-pin SOIC



4.2 20-pin VQFN



5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

VQFN 20-pin	SOIC 20-pin	Pin Name [1,2]	Other/Special	ADC0	PTC[3]	AC0	DAC0	USART0	SPI0	TWI0	TCA0	TCB0	TCD0	CCL
19	16	PA0	$\overline{RESET}$ UPDI	AIN0										LUT0-IN0
20	17	PA1	BREAK	AIN1				TXD	MOSI	SDA				LUT0-IN1
1	18	PA2	EVOUT0	AIN2				RxD	MISO	SCL				LUT0-IN2
2	19	PA3	EXTCLK	AIN3				XCK	SCK		WO3			
3	20	GND												
4	1	VDD												
5	2	PA4		AIN4	X0/Y0			XDIR	$\overline{SS}$		WO4		WOA	LUT0-OUT
6	3	PA5		AIN5	X1/Y1	OUT					WO5	WO	WOB	
7	4	PA6		AIN6	X2/Y2	AINN0	OUT							
8	5	PA7		AIN7	X3/Y3	AINP0								LUT1-OUT
9	6	PB5	CLKOUT	AIN8		AINP1					WO2			
10	7	PB4		AIN9		AINN1					WO1			LUT0-OUT
11	8	PB3	TOSC1					RxD			WO0			
12	9	PB2	TOSC2, EVOUT1					TxD			WO2			
13	10	PB1		AIN10	X4/Y4			XCK		SDA	WO1			
14	11	PB0		AIN11	X5/Y5			XDIR		SCL	WO0			
15	12	PC0							SCK			WO	WOC	
16	13	PC1							MISO				WOD	LUT1-OUT
17	14	PC2	EVOUT2						MOSI					
18	15	PC3							$\overline{SS}$		WO3			LUT1-IN0

Note:

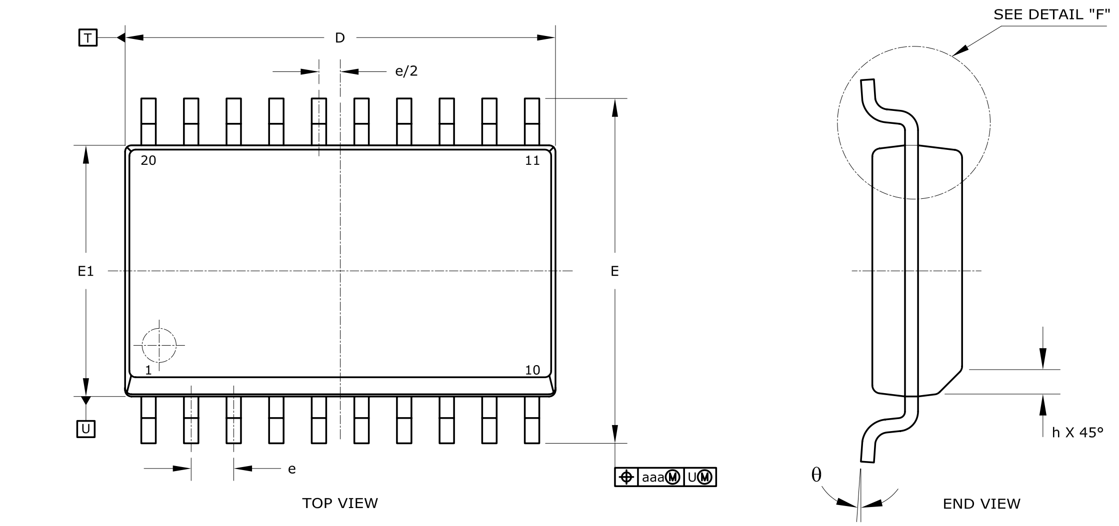
1. Pins names are of type P*xn*, with *x* being the PORT instance (A,B) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.
3. PTC is only available in devices with 8KB Flash (ATtiny816). Every PTC line can be configured as X-line or Y-line.

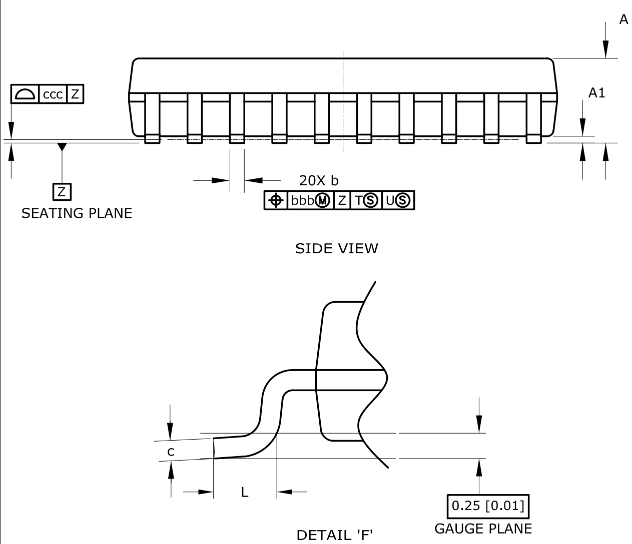
Tip: Signals on alternative pin locations are in `typewriter` font.

6. Package Drawings

6.1 20-pin SOIC

DRAWINGS NOT SCALED





COMMON DIMENSIONS
(Unit of Measure = mm)

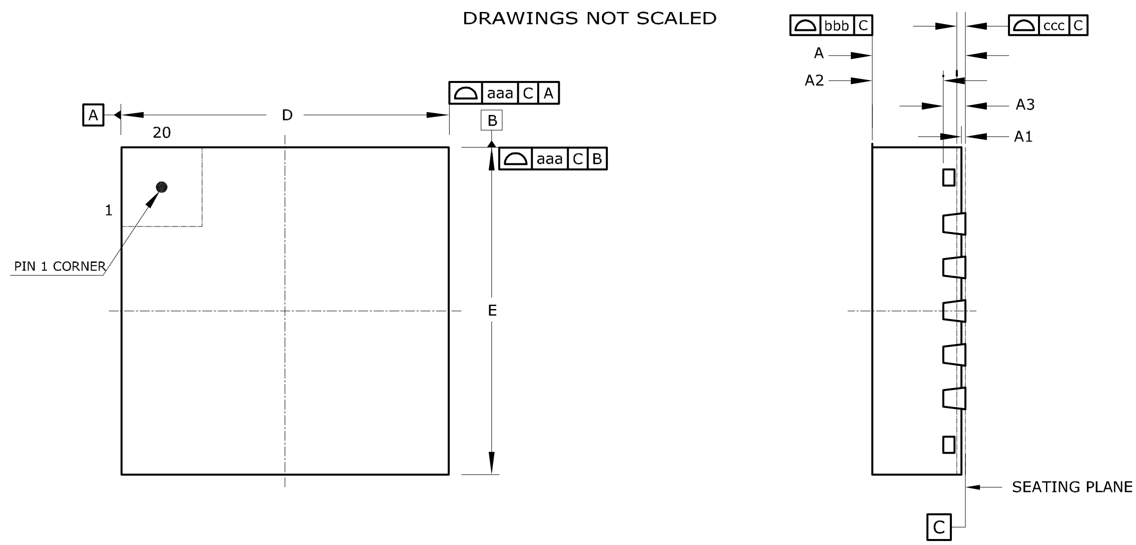
SYMBOL	MIN	NOM	MAX	NOTE
A	2.35	2.50	2.65	
A1	0.10	----	0.30	
D	12.60	12.80	13.00	2
E	10.00	10.30	10.65	
E1	7.40	7.50	7.60	3
L	0.40	----	1.27	
b	0.31	----	0.51	4
c	0.20	----	0.33	
e	1.27 BSC			
h	0.25	----	0.75	
θ	0°	----	8°	
TOLERANCES OF FORM AND POSITION				
aaa	0.25			
bbb	0.25			
ccc	0.10			
n	20			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-013, Variation AC.
2. Dimensions D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions or gate burrs shall not exceed 0.15mm per end.
3. Dimensions E1 does not include inter-lead Flash or protrusion. Inter-lead Flash or protusion shall not exceed 0.25mm per side.
4. Dimensions "b" does not include the Dambar protrusion. Allowable Dambar protrusion shall be 0.10mm total in excess of the "b" dimension maximum material condition. The Dambar may not be located on the lower radius of the foot.

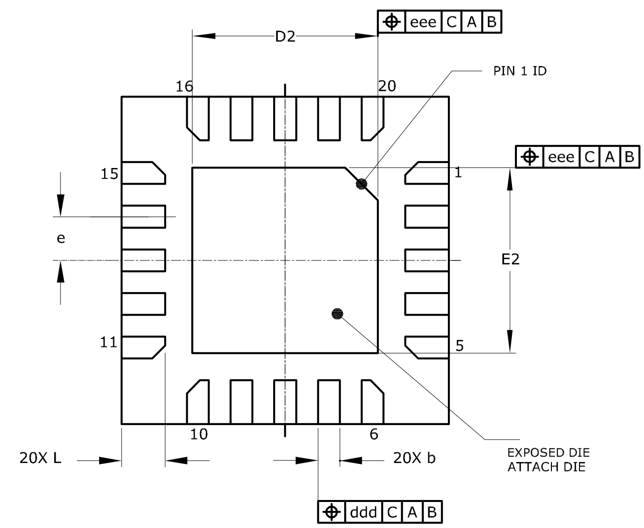
02/05/2014

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	TG, 20 Lds - 1.27mm Pitch, 12.8X7.5x2.50mm Body Size Plastic Small Outline Package (SOIC)	SRJ	TG	P

6.2 20-pin VQFN



TOP VIEW | SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.035	0.05	
A2	-----	0.65	0.67	
A3	0.203 REF			
D/E	3.00 BSC			
D2/E2	1.6	1.7	1.8	
L	0.35	0.40	0.45	
b	0.15	0.20	0.25	2
e	0.4 BSC			
TOLERANCES OF FORM AND POSITION				
aaa	0.100			
bbb	0.100			
ccc	0.08			
ddd	0.100			
eee	0.100			
n	20			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VEEE for proper dimensions, tolerances, datums, etc. (excepted D2/E2).
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

12/18/2015

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	20 Lds - 0.40mm Pitch, 3x3x0.9mm Body size Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZCL	18	A

7. Thermal Considerations

7.1 Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 7-1. Thermal Resistance Data

Package Type	θ_{JA} [°C/W]	θ_{JC} [°C/W]
20-pin SOIC300 (SRJ)	44	21
20-pin VQFN (ZCL)	79.7	36

Related Links

Junction Temperature

7.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

Thermal Resistance Data

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