

INA12x 低功耗精密仪表放大器

1 特性

- 低失调电压：50 μV (最大值)
- 低漂移：0.5 $\mu\text{V}/^\circ\text{C}$ (最大值)
- 低输入偏置电流：5nA (最大值)
- 低噪声：8nV/ $\sqrt{\text{Hz}}$ ，0.2 μV_{pp}
- 高 CMR：120dB (最小值)
- 带宽：1.3 MHz ($G = 1$)
- 输入保护电压可达 $\pm 40\text{V}$
- 宽电源电压范围： $\pm 2.25\text{V}$ 至 $\pm 18\text{V}$
- 低静态电流：700 μA
- 封装：8 引脚塑料 DIP，SO-8

2 应用

- 压力变送器
- 温度变送器
- 称重计
- 心电图 (ECG)
- 模拟输入模块
- 数据采集 (DAQ)

3 说明

INA128 和 INA129 (INA12x) 均为具备出色精度的低功耗通用仪表放大器。这些放大器采用多功能三级运算放大器设计，尺寸小巧，适用于多种应用。即使在高增益 (200kHz、 $G = 100$) 情况下，电流反馈输入电路也可提供宽带宽。

可通过单个外部电阻器在 1 到 10,000 范围内设置任意增益。INA128 可提供具有 50k Ω 电阻的业界通用增益公式。INA129 增益公式使用 49.4k Ω 电阻器，可直接替换同类器件。

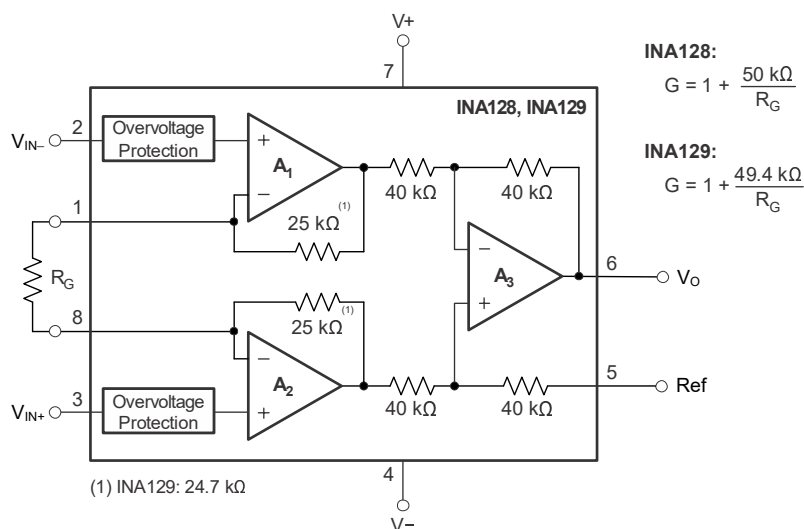
INA12x 采用塑料 DIP 和表面贴装式封装，额定温度范围为 -40°C 至 $+85^\circ\text{C}$ 。INA128 也采用双路配置，即 [INA2128](#)。

升级后的 [INA828](#) 在相同静态电流下可提供更低的输入偏置电流 (最大值 0.6nA)，并且具有更低的噪声 (7nV/ $\sqrt{\text{Hz}}$)。请参阅 [器件比较表](#)，了解如何选择德州仪器 (TI) 提供的精密仪表放大器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
INA128、 INA129	SOIC (8)	3.91mm × 4.90mm
	PDIP (8)	6.35mm × 9.81mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



简化版原理图



Table of Contents

1 特性	1	9.1 Application Information.....	14
2 应用	1	9.2 Typical Application.....	15
3 说明	1	9.3 System Examples.....	19
4 Revision History	2	10 Power Supply Recommendations	21
5 Device Comparison Table	4	10.1 Low-Voltage Operation.....	21
6 Pin Configuration and Functions	4	11 Layout	21
7 Specifications	5	11.1 Layout Guidelines.....	21
7.1 Absolute Maximum Ratings.....	5	11.2 Layout Example.....	21
7.2 ESD Ratings.....	5	12 Device and Documentation Support	22
7.3 Recommended Operating Conditions.....	5	12.1 Device Support.....	22
7.4 Thermal Information.....	5	12.2 Documentation Support.....	22
7.5 Electrical Characteristics.....	6	12.3 接收文档更新通知.....	22
7.6 Typical Characteristics.....	8	12.4 支持资源.....	22
8 Detailed Description	12	12.5 Trademarks.....	22
8.1 Overview.....	12	12.6 Electrostatic Discharge Caution.....	23
8.2 Functional Block Diagram.....	12	12.7 术语表.....	23
8.3 Feature Description.....	13	13 Mechanical, Packaging, and Orderable Information	23
8.4 Device Functional Modes.....	13		
9 Application and Implementation	14		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (April 2019) to Revision F (May 2022)	Page
• 更新了整个文档的表、图和交叉参考的编号格式.....	1
• 在 <i>特性</i> 中添加了带宽和噪声规格.....	1
• 更改了 <i>应用</i> 以链接到 ti.com 上全新的终端设备解决方案.....	1
• Changed reference from INA819 to INA818 in <i>Device Comparison Table</i>	4
• Added single supply specification to <i>Absolute Maximum Ratings</i>	5
• Added note clarifying output short-circuit "to ground" in <i>Absolute Maximum Ratings</i> refers to short-circuit to $V_S / 2$	5
• Added single supply specification to <i>Recommended Operating Conditions</i>	5
• Changed input common-mode voltage range specification from $V - 2$ to $(V -) + 2$ in <i>Recommended Operating Conditions</i>	5
• Deleted INA128-HT and INA129-HT operating temperature specifications from <i>Recommended Operating Conditions</i>	5
• Added specified temperature range to <i>Recommended Operating Conditions</i>	5
• Added $V_{REF} = 0\text{ V}$, $V_{CM} = V_S / 2$, and $G = 1$ to "unless otherwise noted" conditions in <i>Electrical Characteristics</i> and <i>Typical Characteristics</i> for clarity.....	6
• Changed test condition for offset voltage drift specification in <i>Electrical Characteristics</i> from " $T_A = T_{MIN}$ to T_{MAX} " to " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " for clarity.....	6
• Changed typical long-term stability specification from $\pm 0.1 \pm 3/G\text{ }\mu\text{V/mo}$ to $\pm 0.2 \pm 3/G\text{ }\mu\text{V/mo}$ in <i>Electrical Characteristics</i>	6
• Changed common-mode voltage specification from $(V -) + 2\text{ V}$ minimum and $(V+) - 2\text{ V}$ minimum across two rows to $(V -) + 2\text{ V}$ minimum and $(V+) - 2\text{ V}$ maximum across one row in <i>Electrical Characteristics</i>	6
• Deleted typical common-mode voltage specifications in <i>Electrical Characteristics</i>	6
• Added test condition of " $R_S = 0\text{ }\Omega$ " to safe input voltage specification in <i>Electrical Characteristics</i> for clarity.....	6
• Added test condition of " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " to input bias current drift specification in <i>Electrical Characteristics</i> for clarity.....	6

• Added test condition of " $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ " to input offset current drift specification in <i>Electrical Characteristics</i> for clarity.....	6
• Changed maximum gain error specification for INA128PA/UA and INA129PA/UA with $G = 1$ from $\pm 0.01\%$ to $\pm 0.1\%$ in <i>Electrical Characteristics</i>	6
• Added test condition of " $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ " for gain drift in <i>Electrical Characteristics</i> for clarity.....	6
• Changed parameter names from "Voltage - Positive" to "Positive output voltage swing" and from "Voltage - Negative" to "Negative output voltage swing" in <i>Electrical Characteristics</i>	6
• Deleted typical positive and negative output voltage swing specifications in <i>Electrical Characteristics</i>	6
• Added test condition of "Continuous to $V_S / 2$ " to short-circuit current specification in <i>Electrical Characteristics</i> for clarity.....	6
• Changed typical bandwidth specification for $G = 10$ from 700 kHz to 640 kHz in <i>Electrical Characteristics</i>	6
• Changed typical slew rate specification from 4 V/ μs to 1.2 V/ μs in <i>Electrical Characteristics</i>	6
• Changed typical settling time specification for $G = 1$, $G = 10$, and $G = 100$ from 7 μs , 7 μs , and 9 μs respectively to 12 μs , 12 μs , and 12 μs , in <i>Electrical Characteristics</i>	6
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from <i>Electrical Characteristics</i>	6
• Changed Figures 7-1, 7-3, 7-4, 7-9, 7-10, 7-11, 7-16, 7-17, 7-20, 7-21.....	8
• Changed values discussed in <i>Input Common-Mode Range</i> from typical input common-mode voltage range values to maximum and minimum values.....	14
• Changed Figure 9-1 to fix missing text and include reference voltage.....	15
• Added more detailed guidance concerning REF pin in <i>Design Requirements</i>	15
• Changed Figures 9-6, 9-7.....	18
• Changed Figures 9-10 and 9-11 to fix missing text.....	19
• Added <i>Related Documentation</i> links to <i>Device and Documentation Support</i>	22

Changes from Revision D (January 2018) to Revision E (April 2019)	Page
--	-------------

• 添加了有关升级后的新版本 INA828 的信息.....	1
• Added <i>Device Comparison Table</i>	4

Changes from Revision C (October 2015) to Revision D (January 2018)	Page
--	-------------

• 添加了“TI 参考设计”的顶部导航图标.....	1
• Changed " $\pm 0.5 \pm 0/G$ " to " $\pm 0.5 \pm 20/G$ " in MAX column of Offset voltage RTI vs temperature row of <i>Electrical Characteristics</i>	6

Changes from Revision B (February 2005) to Revision C (April 2015)	Page
---	-------------

• 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。.....	1
--	---

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35- μ V offset, 0.4- μ V/ $^{\circ}$ C V_{OS} drift, 8-nV/ $\sqrt{\text{Hz}}$ noise, low-power, precision instrumentation amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA821	35- μ V offset, 0.4- μ V/ $^{\circ}$ C V_{OS} drift, 7-nV/ $\sqrt{\text{Hz}}$ noise, high-bandwidth, precision instrumentation amplifier	$G = 1 + 49.4 \text{ k}\Omega / R_G$	2, 3
INA828	50- μ V offset, 0.5- μ V/ $^{\circ}$ C V_{OS} drift, 7-nV/ $\sqrt{\text{Hz}}$ noise, low-power, precision instrumentation amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA333	25- μ V V_{OS} , 0.1- μ V/ $^{\circ}$ C V_{OS} drift, 1.8-V to 5-V, RRO, 50- μ A I_Q , chopper-stabilized INA	$G = 1 + 100 \text{ k}\Omega / R_G$	1, 8
PGA280	20-mV to ± 10 -V programmable gain IA with 3-V or 5-V differential output; analog supply up to ± 18 V	Digital programmable	N/A
INA159	$G = 0.2$ V differential amplifier for ± 10 -V to 3-V and 5-V conversion	$G = 0.2 \text{ V/V}$	N/A
PGA112	Precision programmable gain op amp with SPI	Digital programmable	N/A

6 Pin Configuration and Functions

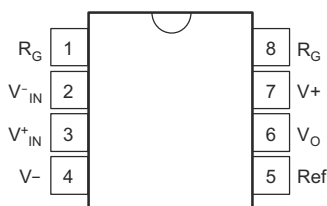


图 6-1. D (8-Pin SOIC) and P (8-Pin PDIP) Packages, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
REF	5	Input	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1,8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V^-	4	Power	Negative supply
V^+	7	Power	Positive supply
V_{IN-}	2	Input	Negative input
V_{IN+}	3	Input	Positive input
V_O	6	Output	Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Dual supply, V _S = (V ₊) - (V ₋)		±18	V
		Single supply, V _S = (V ₊) - 0 V		36	
	Analog input voltage			±40	V
	Output short-circuit ⁽²⁾		Continuous		
T _A	Operating temperature		- 40	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C
T _{stg}	Storage temperature		- 55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V _S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
	Input common-mode voltage range for V _O = 0 V		(V ₋) + 2		(V ₊) - 2	V
T _A	Specified temperature		- 40		85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	110	46.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57	34.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	54	23.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11	11.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V _{OS}	Offset voltage (RTI)	1 ≤ G ≤ 10000	INA12xP, INA12xU		±10 ±100 / G		±50 ±500 / G	μV
			INA12xPA, INA12xUA		±25 ±100 / G ±125 ±1000 / G			
	Offset voltage drift (RTI)	T _A = - 40°C to +85°C	INA12xP, INA12xU		±0.2 ±2 / G		±0.5 ±20 / G	μV/°C
			INA12xPA, INA12xUA		±0.2 ±5 / G ±1 ±20 / G			
PSRR	Power-supply rejection ratio (RTI)	V _S = ±2.25 V to ±18 V	INA12xP, INA12xU		±0.2 ±20 / G		±1 ±100 / G	μV/V
			INA12xPA, INA12xUA		±2 ±200 / G			
	Long-term stability				±0.2 ±3 / G			μV/mo
	Input impedance	Differential		10 2				GΩ pF
		Common-mode		100 9				
V _{CM}	Common-mode voltage ⁽²⁾	V _O = 0 V			(V ⁻) + 2		(V ⁺) - 2	V
	Safe input voltage	R _S = 0 Ω					±40	V
CMRR	Common-mode rejection ratio	Δ R _S = 1 kΩ , V _{CM} = ±13 V	G = 1	INA12xP, INA12xU	80	86	dB	
				INA12xPA, INA12xUA	73			
			G = 10	INA12xP, INA12xU	100	106		
				INA12xPA, INA12xUA	93			
			G = 100	INA12xP, INA12xU	120	125		
				INA12xPA, INA12xUA	110			
			G = 1000	INA12xP, INA12xU	120	130		
				INA12xPA, INA12xUA	110			
INPUT BIAS CURRENT								
I _B	Input bias current	INA12xP, INA12xU			±2		±5	nA
		INA12xPA, INA12xUA					±10	
	Input bias current drift	T _A = - 40°C to +85°C			±30			pA/°C
I _{OS}	Input offset current	INA12xP, INA12xU			±1		±5	nA
		INA12xPA, INA12xUA					±10	nA
	Input offset current drift	T _A = - 40°C to +85°C			±30			pA/°C
NOISE								
e _N	Voltage noise (RTI)	G = 1000, R _S = 0 Ω	f = 10 Hz		10		nV/ √ Hz	
			f = 100 Hz		8			
			f = 1 kHz		8			
			f _B = 0.1 Hz to 10 Hz		0.2		μV _{PP}	
I _n	Current noise	f = 10 Hz		0.9		pA/ √ Hz		
		f = 1 kHz		0.3				
		f _B = 0.1 Hz to 10 Hz		30		pA _{PP}		

7.5 Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, $V_{CM} = V_S / 2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
	Gain equation	INA128		1 + (50 kΩ / R _G)		V/V	
		INA129		1 + (49.4 kΩ / R _G)			
G	Gain			1	10000	V/V	
GE	Gain error	G = 1	INA12xP, INA12xU	±0.01	±0.024	%	
			INA12xPA, INA12xUA	±0.1			
		G = 10	INA12xP, INA12xU	±0.02	±0.4		
			INA12xPA, INA12xUA	±0.5			
		G = 100	INA12xP, INA12xU	±0.05	±0.5		
			INA12xPA, INA12xUA	±0.7			
		G = 1000	INA12xP, INA12xU	±0.5	±1		
			INA12xPA, INA12xUA	±2			
	Gain drift ⁽⁴⁾	T _A = - 40°C to +85°C		±1	±10	ppm/°C	
			50-k Ω or 49.4-k Ω resistance ⁽³⁾	±25	±100		
	Gain nonlinearity ⁽¹⁾	G = 1, V _O = ±13.6 V	INA12xP, INA12xU	±0.0001	±0.001	% of FSR	
			INA12xPA, INA12xUA	±0.002			
		G = 10	INA12xP, INA12xU	±0.0003	±0.002		
			INA12xPA, INA12xUA	±0.004			
		G = 100	INA12xP, INA12xU	±0.0005	±0.002		
			INA12xPA, INA12xUA	±0.004			
		G = 1000			±0.001		
			OUTPUT				
	Positive output voltage swing			(V+) - 1.4		V	
	Negative output voltage swing			(V-) + 1.4		V	
C _L	Load capacitance	Stable operation		1000		pF	
I _{SC}	Short-circuit current	Continuous to V _S / 2		+6/ - 15		mA	
FREQUENCY RESPONSE							
BW	Bandwidth, - 3 dB	G = 1		1.3		MHz	
		G = 10		640		kHz	
		G = 100		200			
		G = 1000		20			
SR	Slew rate	G = 5, V _O = ±10 V		1.2		V/μs	
t _S	Settling time	To 0.01%	G = 1	12		μs	
			G = 10	12			
			G = 100	12			
			G = 1000	80			
	Overload recovery	50% input overload		4		μs	
POWER SUPPLY							
I _Q	Quiescent current	V _{IN} = 0 V		±700		±750	μA

- (1) Nonlinearity measurements in $G = 1000$ are dominated by noise. Typical nonlinearity is $\pm 0.001\%$
- (2) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
- (3) Temperature coefficient of the 50-k Ω or 49.4-k Ω term in the gain equation.
- (4) Specified by wafer test.

7.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ (unless otherwise noted)

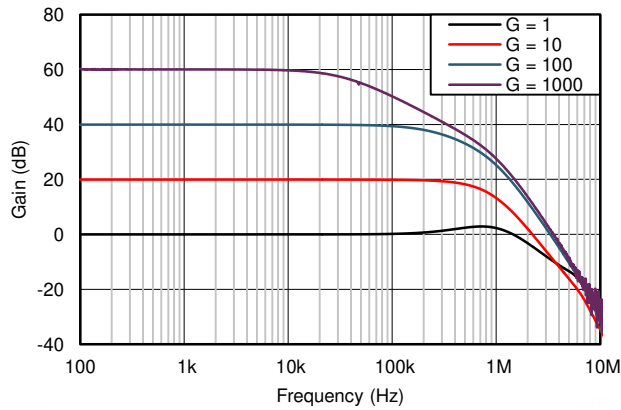


图 7-1. Gain vs Frequency

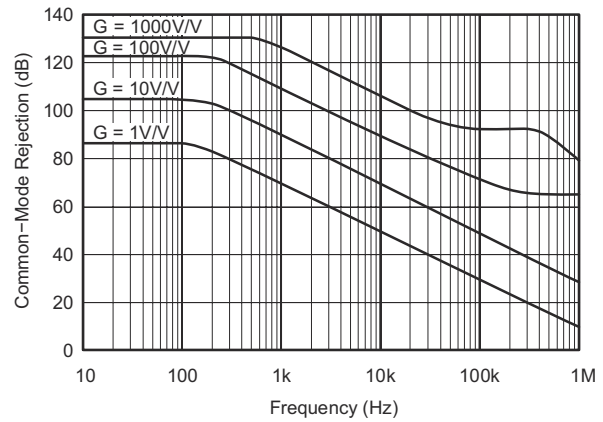


图 7-2. Common-Mode Rejection vs Frequency

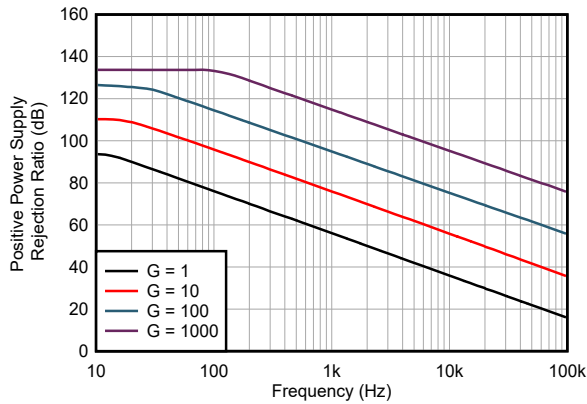


图 7-3. Positive Power Supply Rejection vs Frequency

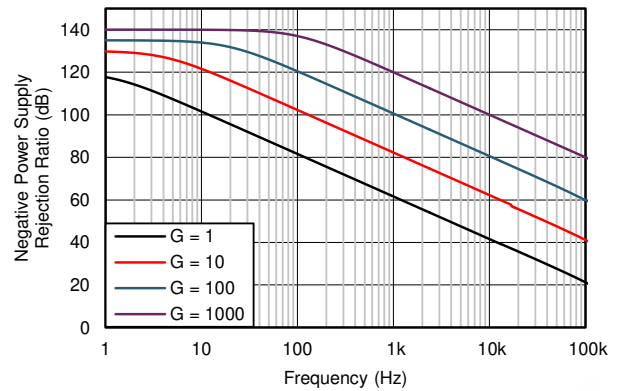


图 7-4. Negative Power Supply Rejection vs Frequency

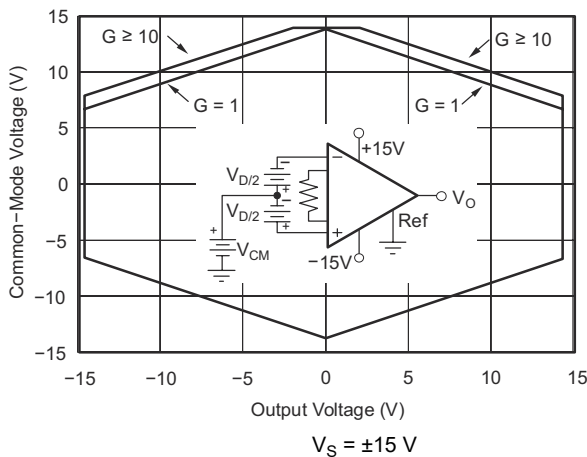


图 7-5. Input Common-Mode Range vs Output Voltage

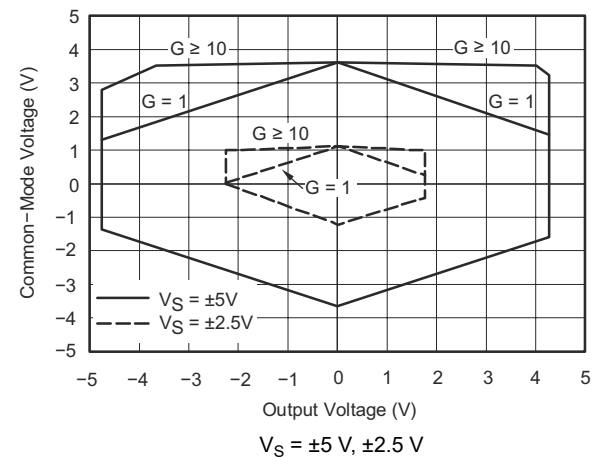


图 7-6. Input Common-Mode Range vs Output Voltage

7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ (unless otherwise noted)

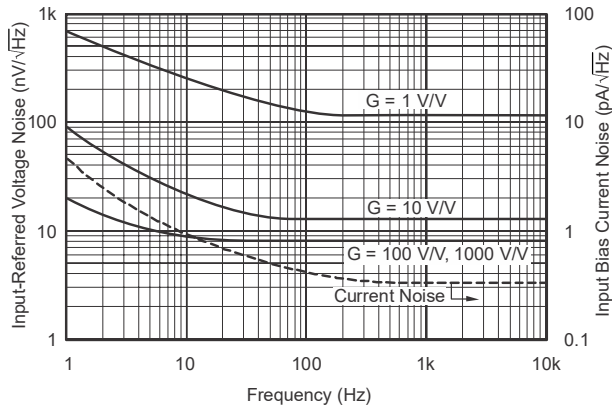


图 7-7. Input-Referred Noise vs Frequency

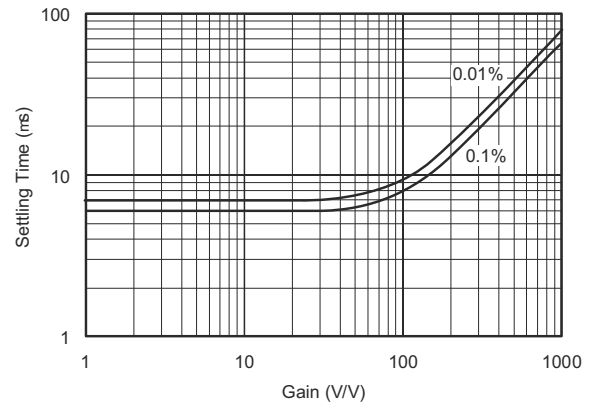


图 7-8. Settling Time vs Gain

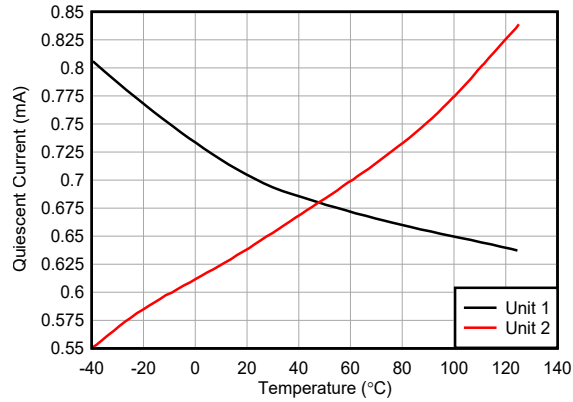


图 7-9. Quiescent Current vs Temperature

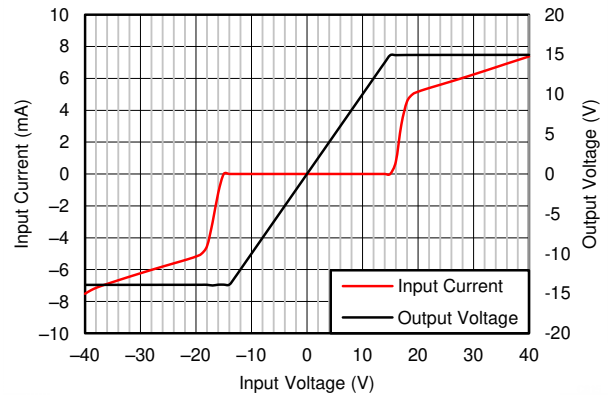


图 7-10. Input Overvoltage V/I Characteristics

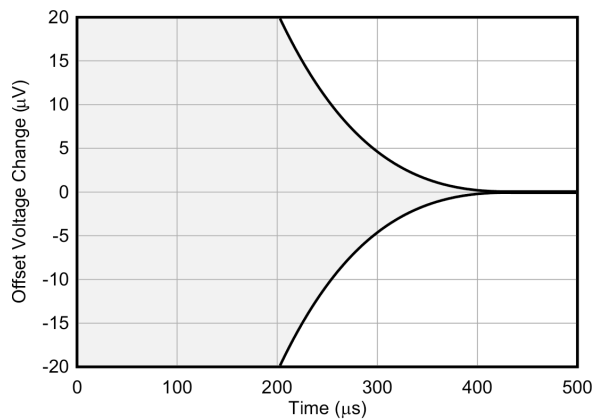


图 7-11. Input Offset Voltage Warm-Up

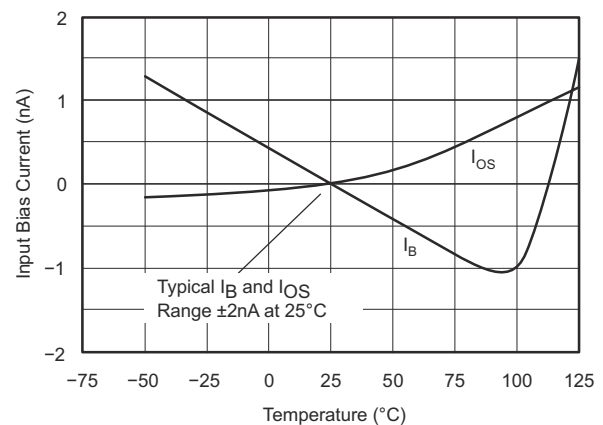


图 7-12. Input Bias Current vs Temperature

7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ (unless otherwise noted)

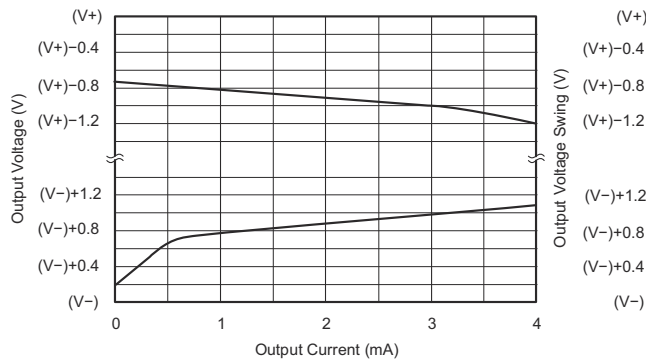


图 7-13. Output Voltage Swing vs Output Current

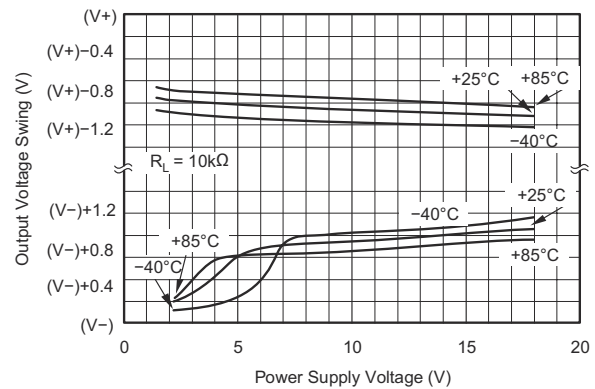


图 7-14. Output Voltage Swing vs Power Supply Voltage

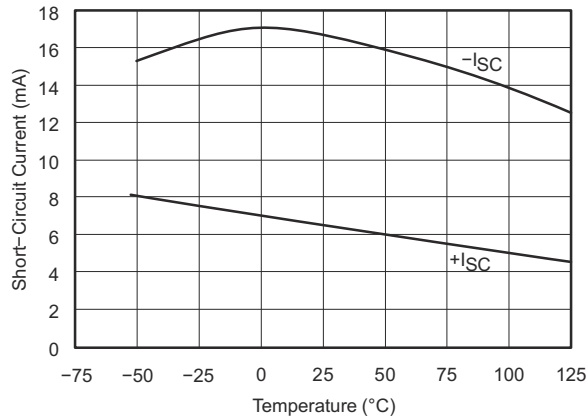


图 7-15. Short-Circuit Output Current vs Temperature

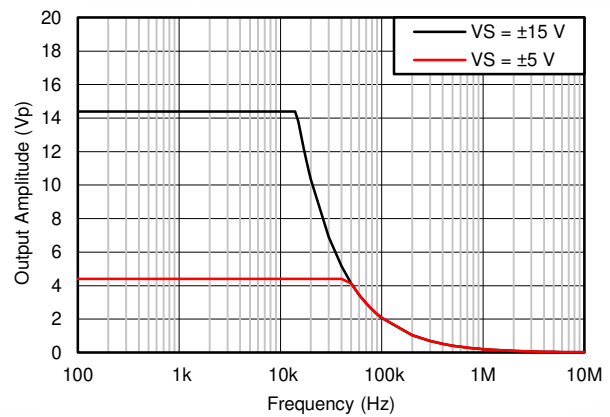


图 7-16. Maximum Output Voltage vs Frequency

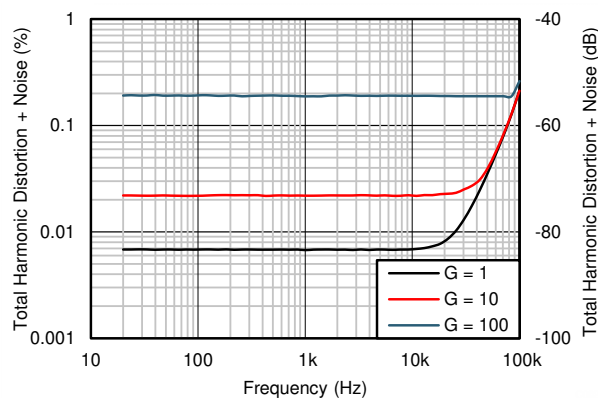


图 7-17. Total Harmonic Distortion + Noise vs Frequency

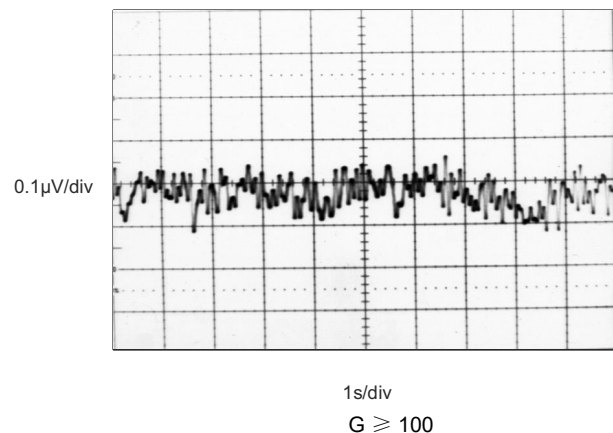


图 7-18. 0.1 to 10-Hz Input-Referred Voltage Noise

7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ (unless otherwise noted)

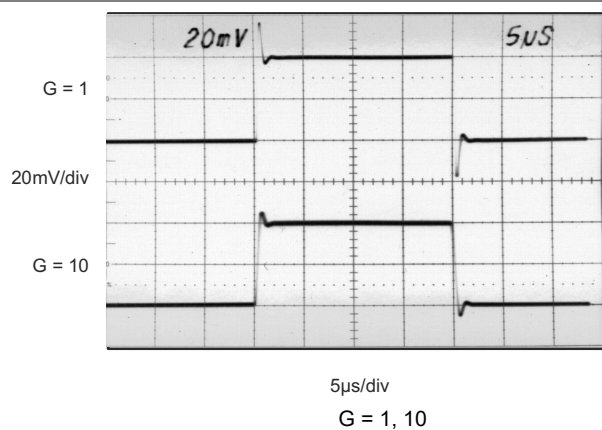


图 7-19. Small Signal

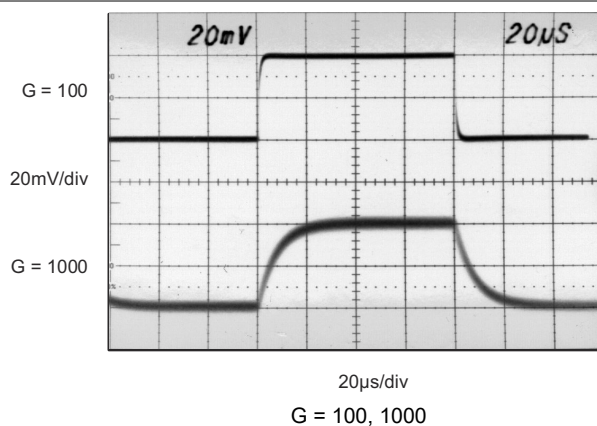


图 7-20. Small Signal

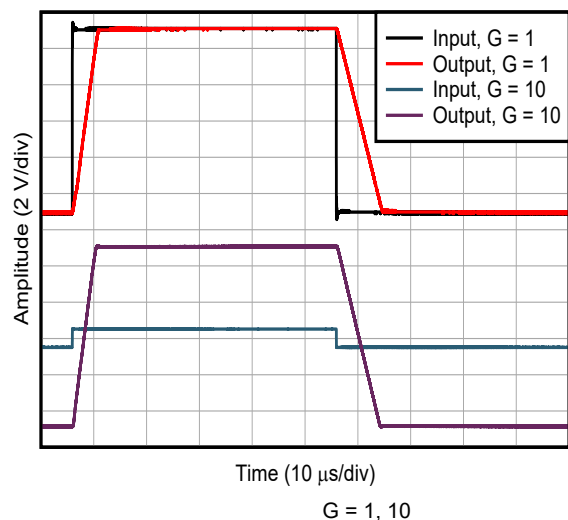


图 7-21. Large Signal

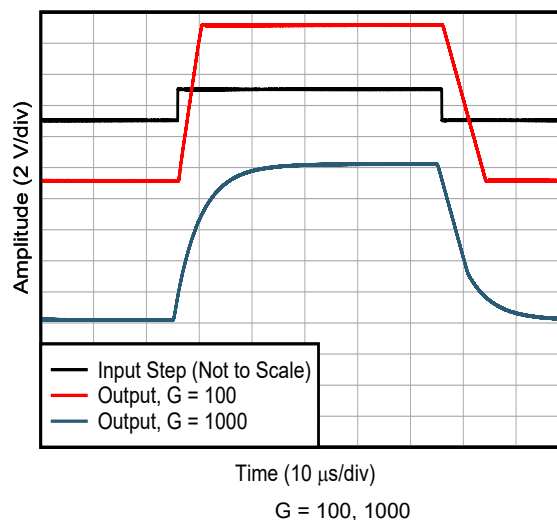


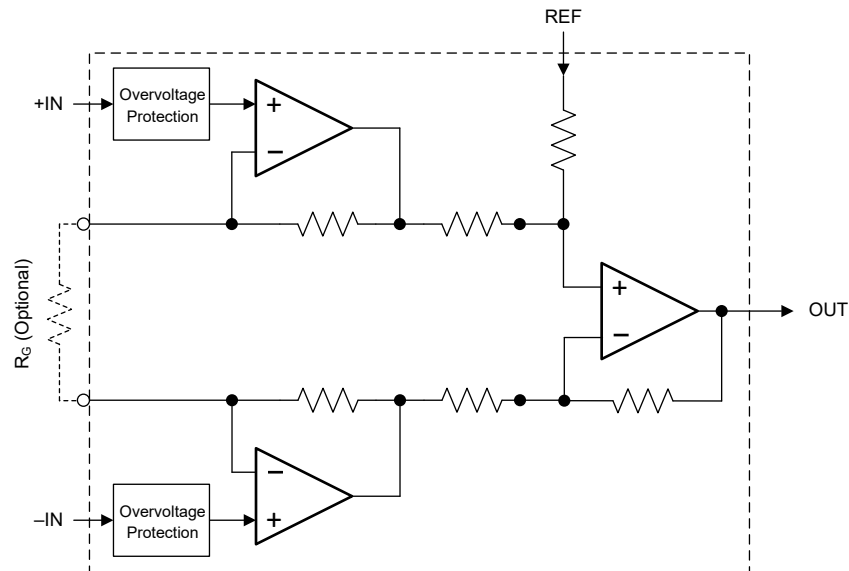
图 7-22. Large Signal

8 Detailed Description

8.1 Overview

The INA128 and INA129 (INA12x) instrumentation amplifiers are outfitted with an input protection circuit and input buffer amplifiers. These features eliminate the need for input impedance matching and make the amplifier an excellent choice for use in measurement and test equipment. Additional characteristics of the INA12x include a very-low dc offset, low drift, low noise, very-high open-loop gain, very-high common-mode rejection ratio, and very-high input impedances. The INA12x is used where great accuracy and stability of the circuit, both short and long term, are required.

8.2 Functional Block Diagram



8.3 Feature Description

The INA12x are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-op-amp design and small size make the amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA12x are laser trimmed for very low offset voltage (25 μV typical) and high common-mode rejection (93 dB at $G \geq 100$). These devices operate with power supplies as low as $\pm 2.25\text{ V}$, and a quiescent current of 2 mA, typically. The internal input protection can withstand up to $\pm 40\text{ V}$ without damage, as shown in 图 7-10.

8.3.1 Noise Performance

The INA12x provide very low noise in most applications. Low-frequency noise is approximately $0.2\text{ }\mu\text{V}_{\text{PP}}$ measured from 0.1 to 10 Hz ($G \geq 100$). This feature provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

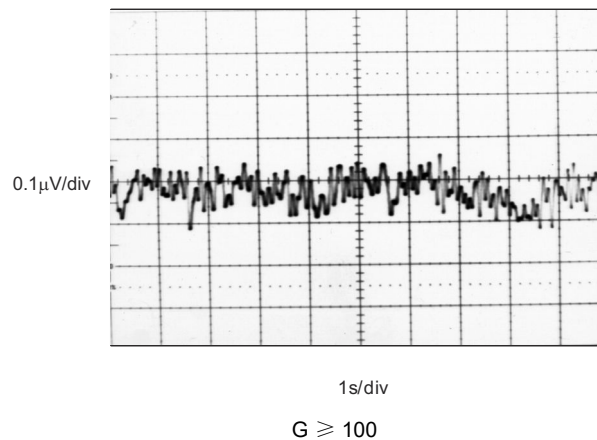


图 8-1. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

8.4 Device Functional Modes

The INA12x have a single functional mode and operate when the power-supply voltage is greater than 4.5 V ($\pm 2.25\text{ V}$). The maximum power-supply voltage for the INA12x is 36 V ($\pm 18\text{ V}$).

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The INA12x measure a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high input-voltage protection circuit in conjunction with high input impedance make the INA12x an excellent choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

9.1.1 Input Common-Mode Range

The linear input voltage range of the INA12x input circuitry ranges from approximately 2 V less than the positive supply voltage to 2 V greater than the negative supply. A differential input voltage causes the output voltage to increase; however, the linear input range is limited by the output voltage swing of amplifiers A₁ and A₂. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on the supply voltage (see [图 7-6](#)).

Input overload can produce an output voltage that appears normal. For example, if an input-overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of A₃ is near 0 V even though both inputs are overloaded.

9.2 Typical Application

图 9-1 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 8 Ω in series with the REF pin causes a typical device to degrade to approximately 80 dB CMR ($G = 1$).

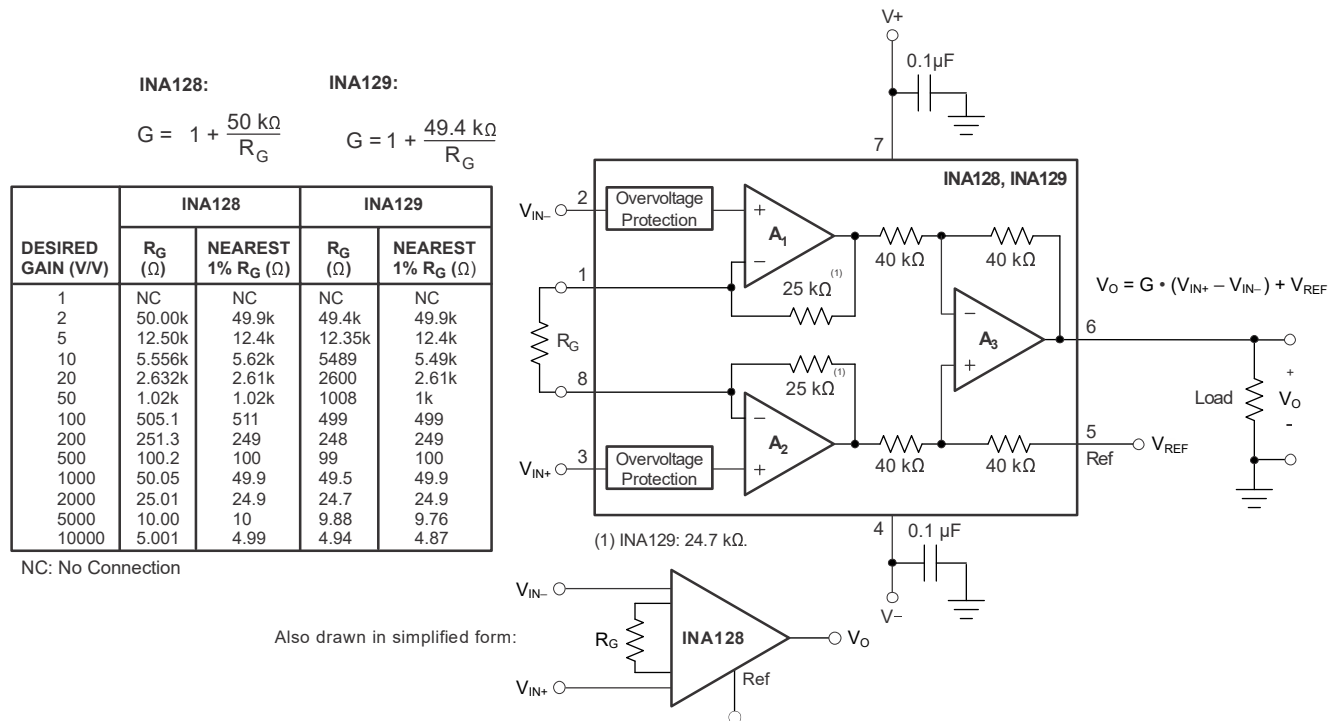


图 9-1. Basic Connections

9.2.1 Design Requirements

The devices are configured to monitor the input differential voltage when the input signal gain is set by the external resistor, R_G . The output signal is developed with respect to the voltage on the reference pin, REF. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground, as 图 9-1 shows. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level shift the output so that the device can drive a single-supply ADC.

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider is used to generate a reference voltage, the voltage must be buffered by an op amp to avoid CMRR degradation.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

The gain (G) is set by connecting a single external resistor, R_G , between pins 1 and 8:

$$\text{INA128: } G = 1 + 50 \text{ k}\Omega / R_G \quad (1)$$

$$\text{INA129: } G = 1 + 49.4 \text{ k}\Omega / R_G \quad (2)$$

Commonly used gains and resistor values are shown in 图 9-1.

The 50-k Ω term in 方程式 1 and the 49.4-k Ω term in 方程式 2 come from the sum of the two internal feedback resistors of A_1 and A_2 . These on-chip metal film resistors are laser trimmed to accurate, absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications in the *Electrical Characteristics* table.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from 方程式 1 and 方程式 2. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

The typical performance curve in 图 7-1 shows that despite low quiescent current, the INA12x achieve wide bandwidth even at high gain. This performance is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

9.2.2.3 Offset Trimming

The INA12x is laser trimmed for low-offset voltage and low offset voltage drift. Most applications require no external offset adjustment. 图 9-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed with the output. The op-amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.

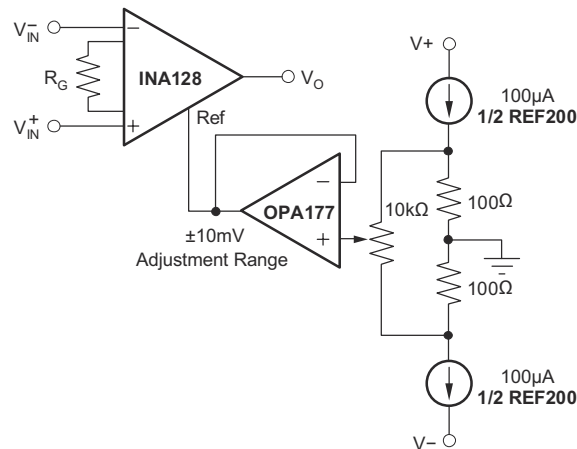


图 9-2. Optional Trimming of Output Offset Voltage

9.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately $10\text{ G}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 2\text{ nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 图 9-3). With higher source impedance, use two equal resistors to provide a balanced input, with possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

For more details about why a valid input bias current return path is necessary, see the [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications](#) application note.

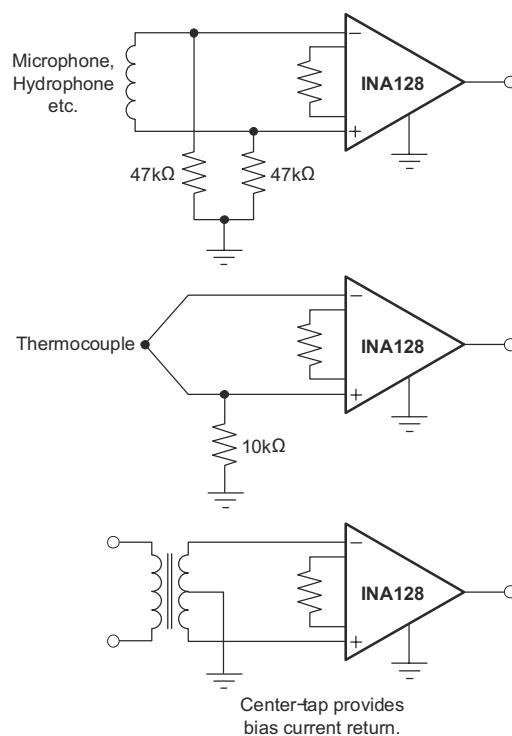


图 9-3. Providing an Input Common-Mode Current Path

9.2.3 Application Curves

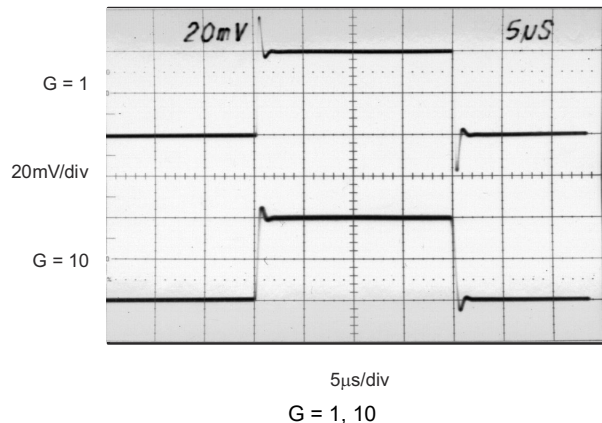


图 9-4. Small Signal

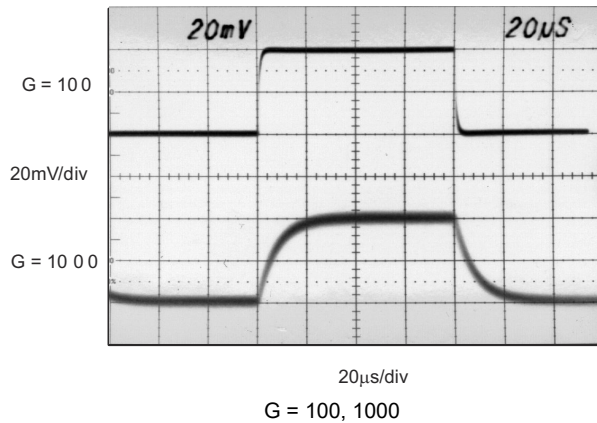


图 9-5. Small Signal

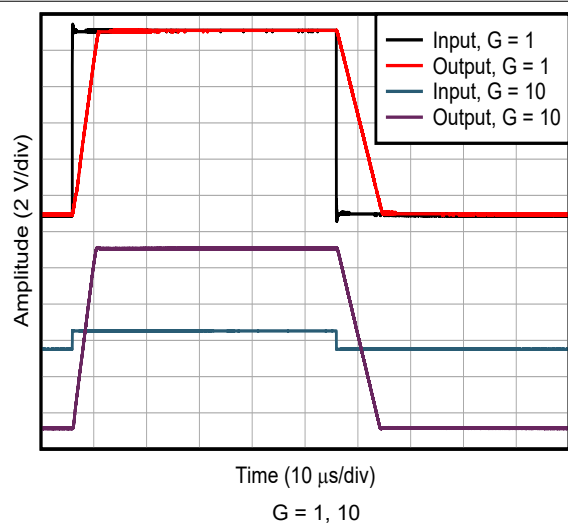


图 9-6. Large Signal

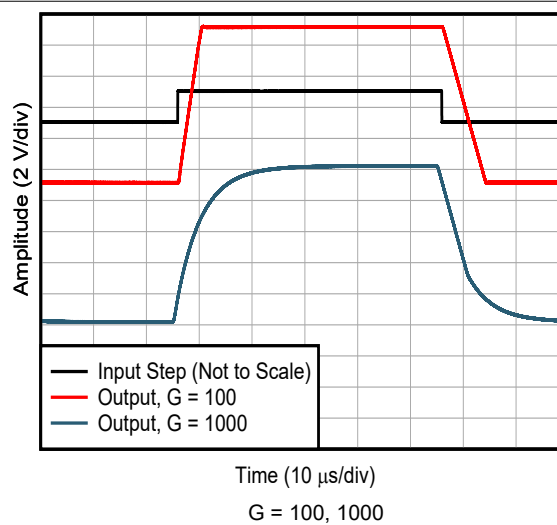


图 9-7. Large Signal

9.3 System Examples

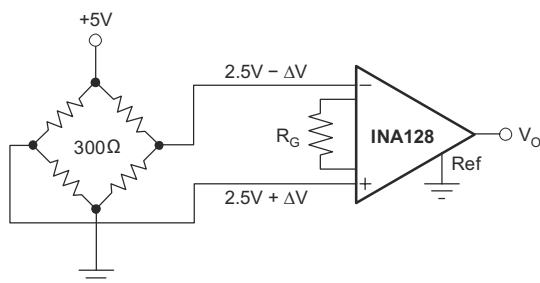


图 9-8. Bridge Amplifier

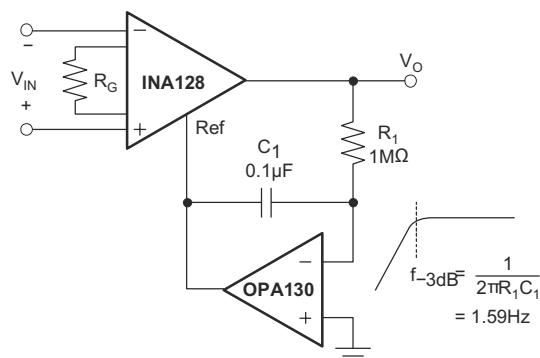
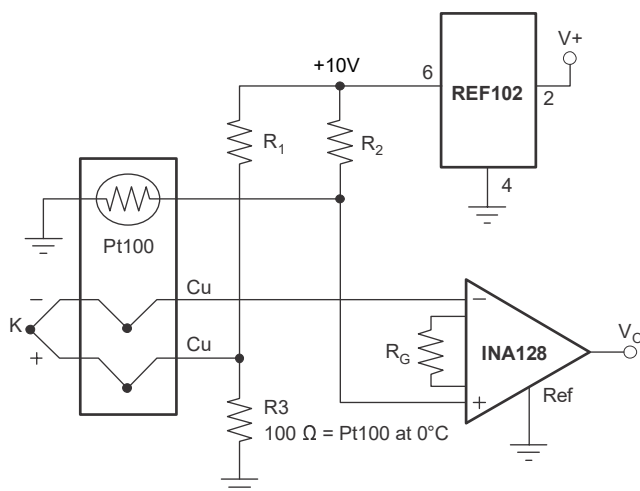


图 9-9. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R1, R2
E	+ Chromel - Constantan	58.5	66.5 kΩ
J	+ Iron - Constantan	50.2	76.8 kΩ
K	+ Chromel - Alumel	39.4	97.6 kΩ
T	+ Copper - Constantan	38.0	102 kΩ

图 9-10. Thermocouple Amplifier With RTD Cold-Junction Compensation

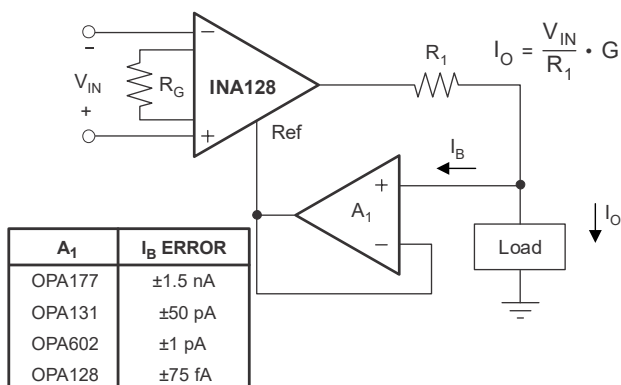


图 9-11. Differential Voltage to Current Converter

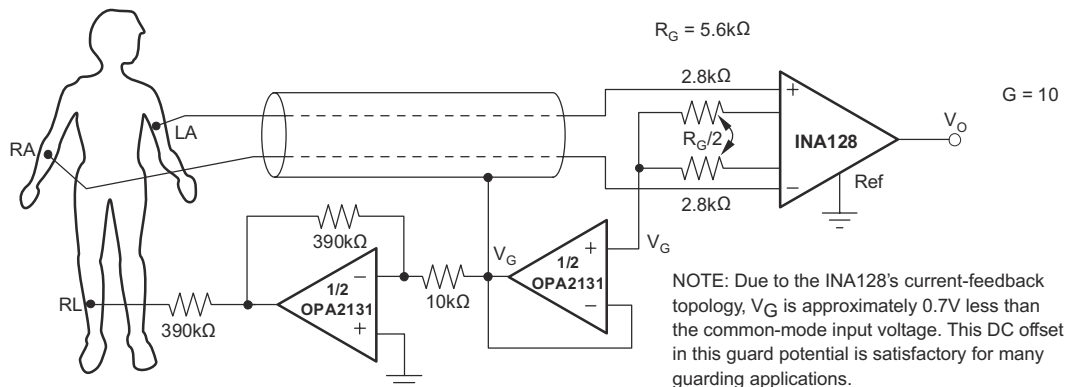


图 9-12. ECG Amplifier With Right-Leg Drive

10 Power Supply Recommendations

The minimum power supply voltage for INA12x is ± 2.25 V and the maximum power supply voltage is ± 18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ± 15 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10.1 Low-Voltage Operation

The INA12x operate on power supplies as low as ± 2.25 V. Performance remains excellent with power supplies ranging from ± 2.25 V to ± 18 V. Most parameters vary only slightly throughout this supply voltage range; see [7.6](#).

Operation at very-low supply voltages requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. [图 7-6](#) shows the range of linear operation for ± 15 -V, ± 5 -V, and ± 2.5 -V supplies.

11 Layout

11.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is $0.1 \mu\text{F}$ to $1 \mu\text{F}$. If necessary, add more decoupling capacitance to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the devices.

11.2 Layout Example

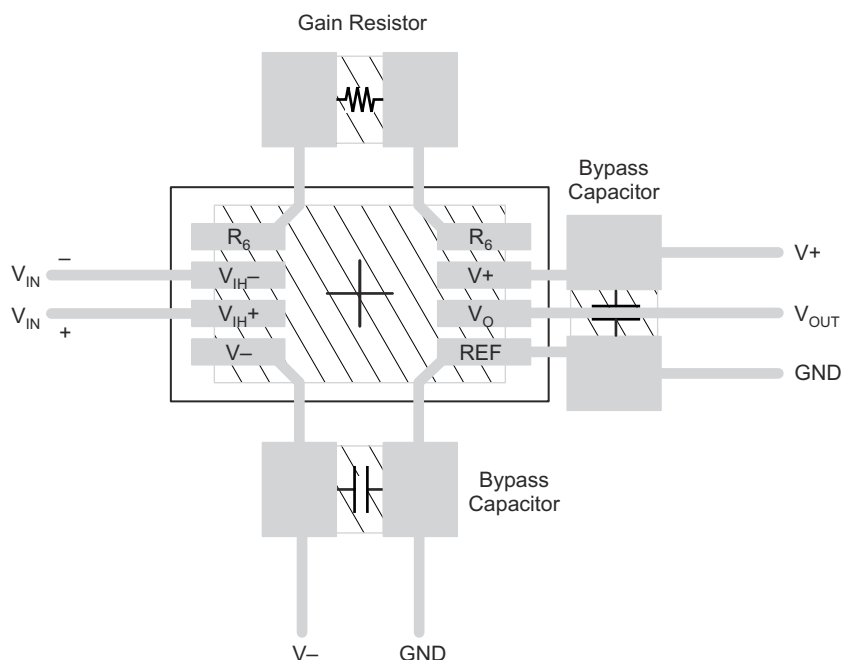


图 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers](#) application note
- Texas Instruments, [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications](#) application note

12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.

TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA128P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	Samples
INA128PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P A	Samples
INA128PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	Samples
INA128U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA128UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA129P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples
INA129PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										A	
INA129PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples
INA129U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-3-260C-168 HR		INA 129U S	Samples
INA129U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-3-260C-168 HR		INA 129U S	Samples
INA129UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA128, INA129 :

- Enhanced Product : [INA129-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA128U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA128UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA128UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA129UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA128P	P	PDIP	8	50	506	13.97	11230	4.32
INA128PA	P	PDIP	8	50	506	13.97	11230	4.32
INA128PG4	P	PDIP	8	50	506	13.97	11230	4.32
INA128U	D	SOIC	8	75	506.6	8	3940	4.32
INA128U	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA	D	SOIC	8	75	506.6	8	3940	4.32
INA128UAE4	D	SOIC	8	75	506.6	8	3940	4.32
INA128UAG4	D	SOIC	8	75	506.6	8	3940	4.32
INA128UG4	D	SOIC	8	75	506.6	8	3940	4.32
INA128UG4	D	SOIC	8	75	506.6	8	3940	4.32
INA129P	P	PDIP	8	50	506	13.97	11230	4.32
INA129PA	P	PDIP	8	50	506	13.97	11230	4.32
INA129PG4	P	PDIP	8	50	506	13.97	11230	4.32
INA129U	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA	D	SOIC	8	75	506.6	8	3940	4.32
INA129UAE4	D	SOIC	8	75	506.6	8	3940	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司