3A Bus Termination Regulator

Features

- Provide Bi-direction Current
  - Sourcing or Sinking Current up to 3A
- 1.25V/0.9V Output for DDR I/II Applications
- Fast Transient Response
- High Output Accuracy
  - ±20mV over Load, VOUT Offset and Temperature
- Adjustable Output Voltage by External Resistors
- Current-Limit Protection
- On-Chip Thermal Shutdown
- Shutdown for Standby or Suspend Mode
- Simple SOP-8, SOP-8-P with thermal pad, TO-252- 5 and TO-263-5 Packages
- Lead Free Available (RoHS Compliant)

Applications

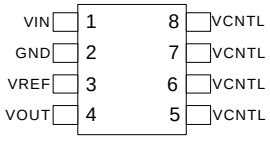
- DDR I/II SDRAM Termination
- SSTL-2/3 Termination Voltage
- Applications Requiring the Regulator with Bi-direction 3A Current Capability

General Description

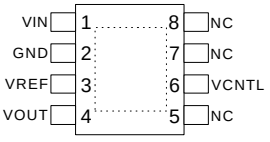
The APL5331 linear regulator is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The APL5331 integrates two power transistors to source or sink current up to 3A. It also incorporate current-limit, thermal shutdown and shutdown control functions into a single chip.

Current-limit circuit limits the short-circuit current. On-chip thermal shutdown provides protection against any combination of overload that would create excessive junction temperature. The output voltage of APL5331 tracks the voltage at VREF pin. A resistor divider connected to VIN, GND and VREF pins is used to provide a half voltage of VIN to VREF pin. In addition, an external ceramic capacitor and an open-drain transistor connected to VREF pin provide soft-start and shutdown control respectively. Pulling and holding the VREF voltage to 0V shuts off the output. The output of APL5331 will be high impedance in shut-down condition.

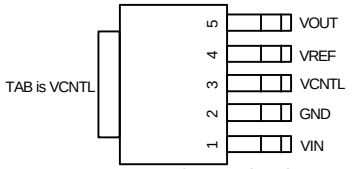
Pin Configuration



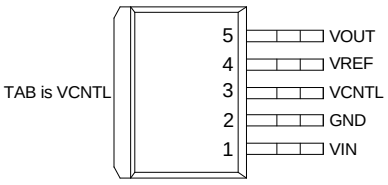
SOP-8 (Top View)



SOP-8-P (Top View)



TO-252-5 (Top View)



TO-263-5 (Top View)

NC = No internal connection

= Thermal Pad (connected to GND plane for better heat dissipation)

Ordering and Marking Information

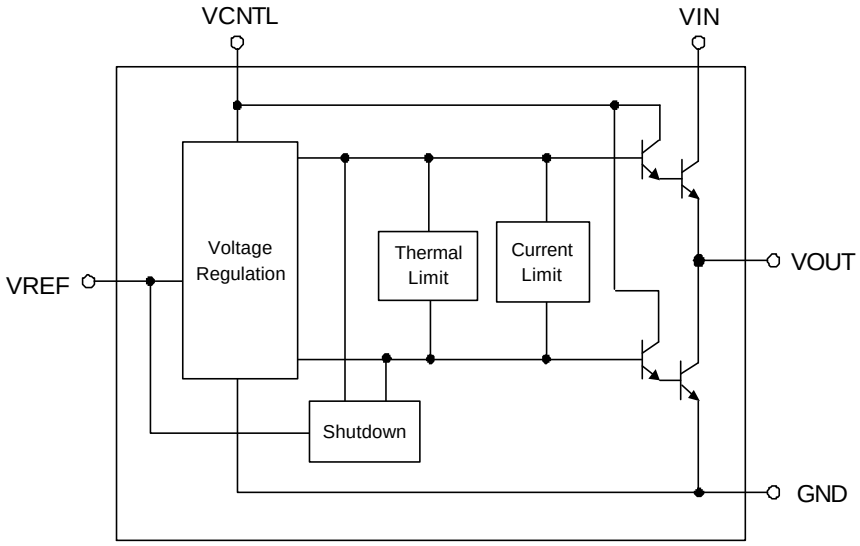
APL5331 □□□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code K : SOP-8 KA : SOP-8-P U5 : TO-252-5 G5 : TO-263-5 Operating Ambient Temp. Range C : 0 to 70 °C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APL5331KC-TR : APL5331KAC-TR :	APL5331 XXXXX XXXXX - Date Code
APL5331U5C-TR : APL5331G5C-TR :	APL5331 XXXXX XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Description

PIN NAME	I/O	DESCRIPTION
VIN	I	Main power input pin. Connect this pin to a voltage source and an input capacitor. The APL5331 sources current to VOUT pin by controlling the upper NPN pass transistor, providing a current path from VIN pin.
GND	O	Power and signal ground. Connect this pin to system ground plane with shortest traces. The APL5331 sinks current from VOUT pin by controlling the lower NPN pass transistor, providing a current path to GND pin. This pin is also the ground path for internal control circuitry.
VCNTL	I	Power input pin for internal control circuitry. Connect this pin to a voltage source, providing a bias for the internal control circuitry. A bypass capacitor is usually connected near this pin.
VREF	I	Reference voltage input and active-low shutdown control pin. Apply a voltage to this pin as a reference voltage for the APL5331. Connect this pin to a resistor divider, between VIN and GND, and a capacitor for soft-start and filtering noise purposes. Applying and holding this VREF voltage low by an open-drain transistor to shut down the output.
VOUT	O	Output pin of the regulator. Connect this pin to load. The output capacitors connected to this pin improve stability and transient response. The output voltage tracks the reference voltage and is capable of sourcing or sinking current up to 3A.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage, VCNTL to GND	-0.2 ~ 7	V
V_{IN}	VIN Supply Voltage, VIN to GND	-0.2 ~ 3.9	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature, 10 Seconds	300	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode)	±3	kV

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air		°C/W
	SOP-8	75	
	SOP-8-P	55	
	TO-252-5	42	
	TO-263-5	34	
θ_{JC}	Junction-to-Case Thermal Resistance		°C/W
	SOP-8	28	
	SOP-8-P	20	
	TO-252-5	12	
	TO-263-5	11	

Note : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8-P is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage (Note 1)	3.1 ~ 6	V
V_{IN}	VIN Supply Voltage (Note 2)	1.2 ~ 3.5	V
V_{OUT}	VOUT Output Voltage (Note 3)	V_{REF} ± 0.02	V
I_{OUT}	VOUT Output Current (Note 4,5)	-3 ~ +3	A
T_J	Junction Temperature	0 ~ 125	°C

Notes :

1. Please refer to the VCNTL-to-VIN Dropout Voltage in the "Typical Characteristics" section for the minimum supply voltage on VCNTL.
2. Please supply enough voltage to VIN for sourcing desired maximum output current. Please refer to the VIN. Dropout Voltage vs Output Current in the Typical Characteristics.
3. The VOUT is regulated to the V_{REF} with additional voltage offset and load regulation except over-load conditions.
4. The symbol "+" means the VOUT sources current to load; the symbol "-" means the VOUT sinks current to to GND.
5. The max. I_{OUT} varies with the T_J and the voltages of V_{IN}-V_{OUT} and V_{OUT}. Please refer to the Typical Characteristics.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over, V_{CNTL}=3.3V, V_{IN}=2.5V/1.8V, V_{REF}=0.5V_{IN} and T_A= 0 to 70°C, unless otherwise specified. Typical values refer to T_A = 25°C.

Symbol	Parameter	Test Conditions	APL5331			Unit
			Min	Typ	Max	
OUTPUT VOLTAGE						
V_{OUT}	VOUT Output Voltage	I_{OUT} = 0A		V_{REF}		V
	System Accuracy	Over temperature, VOUT offset, and load regulation	-20		20	mV
V_{OS}	VOUT Offset Voltage (VOUT–VREF)	I_{OUT} = +10mA	-15	-8		mV
		I_{OUT} = -10mA		6	14	
	Load Regulation	I_{OUT} = +10mA to +3A	-8	-3		mV
		I_{OUT} = -10mA to -3A		1	6	
PROTECTION						
I_{LIM}	Current Limit	Sourcing Current (V_{IN} = 2.5V) T_J = 25°C	+3.3	+3.6		A
		Sourcing Current (V_{IN} = 2.5V) T_J = 125°C		+3.1		
		Sourcing Current (V_{IN} = 2.5V) T_J = 25°C	-3.3	-3.6		
		Sourcing Current (V_{IN} = 2.5V) T_J = 125°C		-3.1		
		Sourcing Current (V_{IN} = 1.8V) T_J = 25°C	+2.9	+3.2		
		Sourcing Current (V_{IN} = 1.8V) T_J = 125°C		+2.6		
		Sourcing Current (V_{IN} = 1.8V) T_J = 25°C	-2.9	-3.2		
		Sourcing Current (V_{IN} = 1.8V) T_J = 125°C		-2.6		
T_{SD}	Thermal Shutdown Temperature	Rising T_J		183		°C
	Thermal Shutdown Hysteresis			42		°C

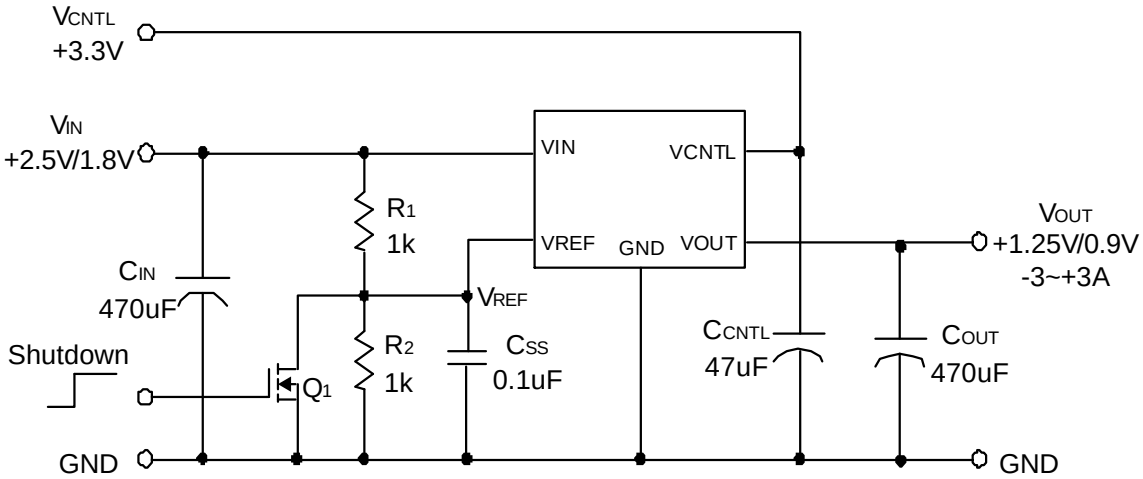
Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over, V_{CNTL}=3.3V, V_{IN}=2.5V/1.8V, V_{REF}=0.5V_{IN} and T_A= 0 to 70°C, unless otherwise specified. Typical values refer to T_A = 25°C.

Symbol	Parameter	Test Conditions	APL5331			Unit
			Min	Typ	Max	
INPUT CURRENT						
I_{CNTL}	VCNTL Supply Current	I_{OUT} = 0A	2	3.9	6	mA
		I_{OUT} = ±3A (Normal Operation)		50	110	
		VREF = GND (Shutdown)		2.0		
I_{VREF}	VREF Bias Current (The current flows out of VREF)	V_{REF} = 1.25V/0.9V (Normal operation)		200	500	nA
		VREF = GND (Shutdown)		20	40	µA
SHUTDOWN CONTROL						
	Shutdown Threshold Voltage		0.2	0.35	0.65	V

Typical Application Circuit

1. V_{OUT}=1.25V/0.9V Application



C_{OUT} : 470µF, ESR=25mΩ

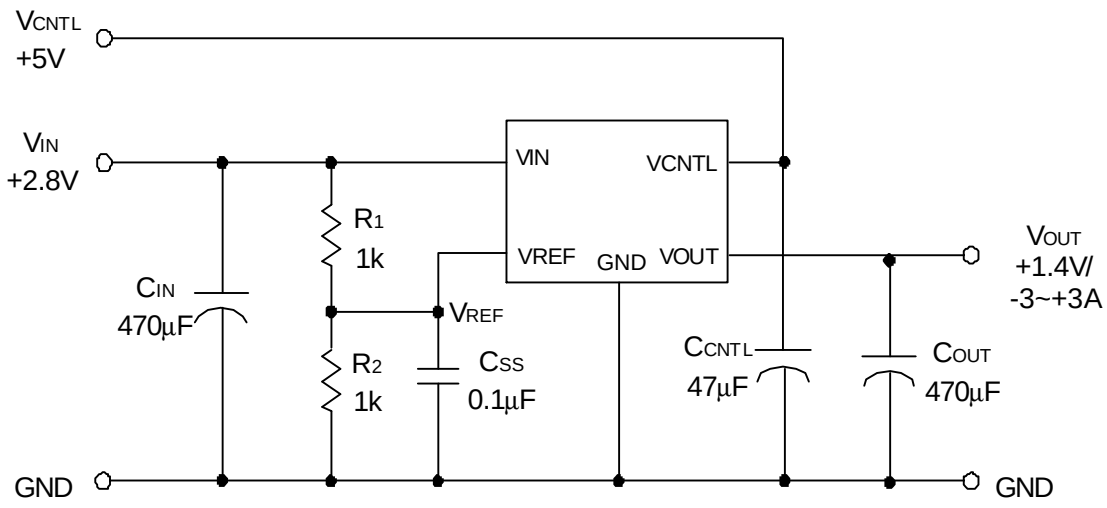
R1, R2 : 1kΩ, 1%

Q1 : APM2300 AC

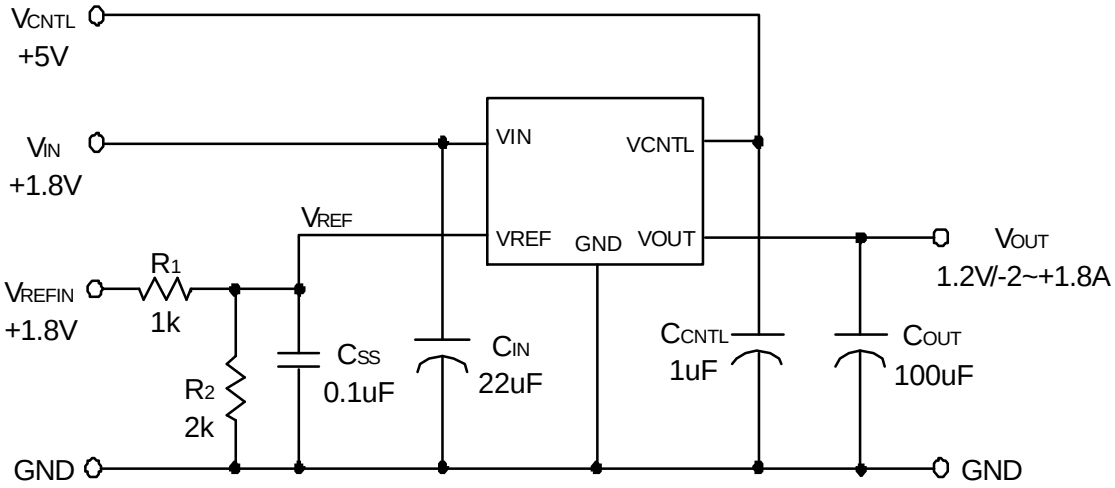
Note : Since R_1 and R_2 are very small, the voltage offset caused by the bias current of VREF can be ignore.

Typical Application Circuit

2. V_{OUT}=1.4V Application



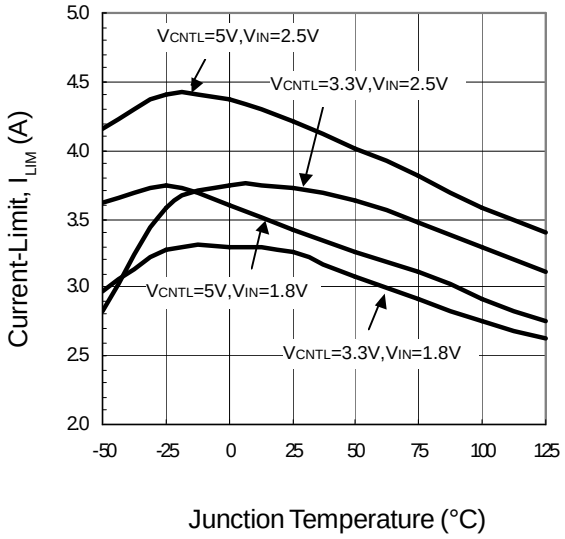
3. General Application



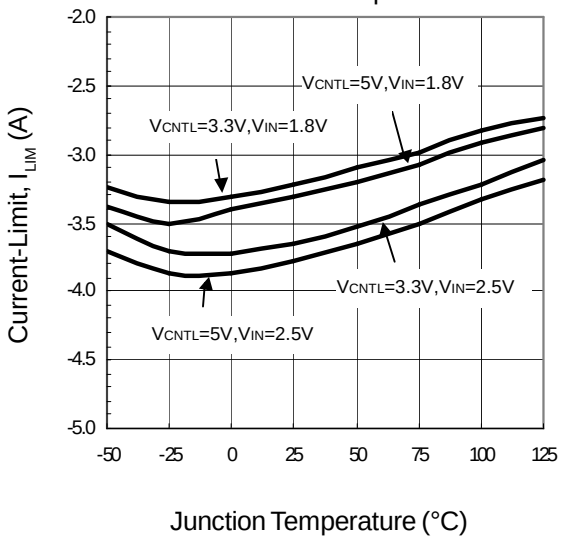
$$V_{OUT} = V_{REFIN} \cdot \frac{R_2}{R_1 + R_2} \quad (V)$$

Typical Characteristics

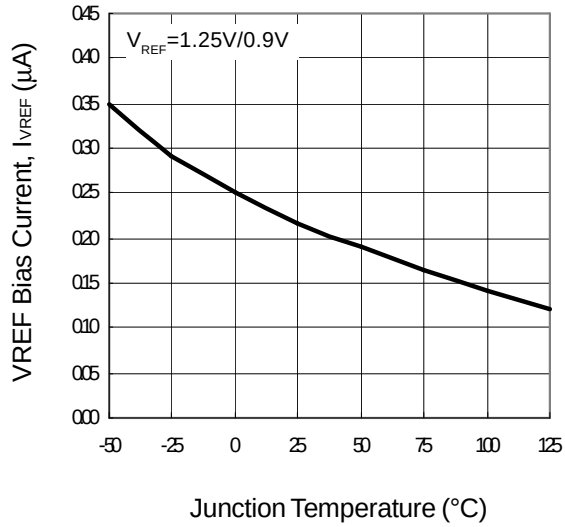
Sourcing Current-Limit
vs Junction Temperature



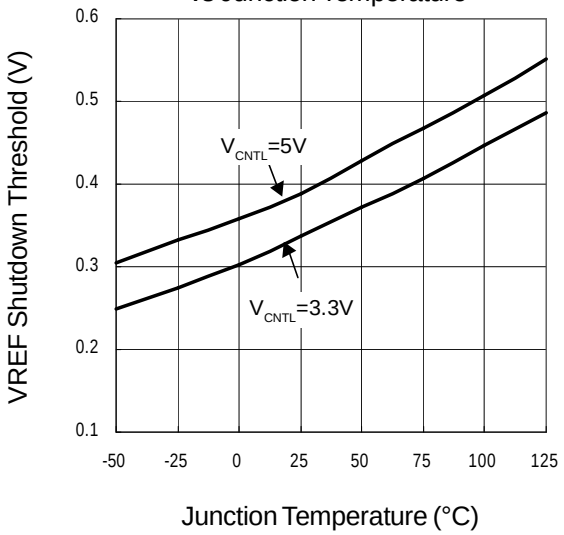
Sinking Current-Limit
vs Junction Temperature



VREF Bias Current
vs Junction Temperature

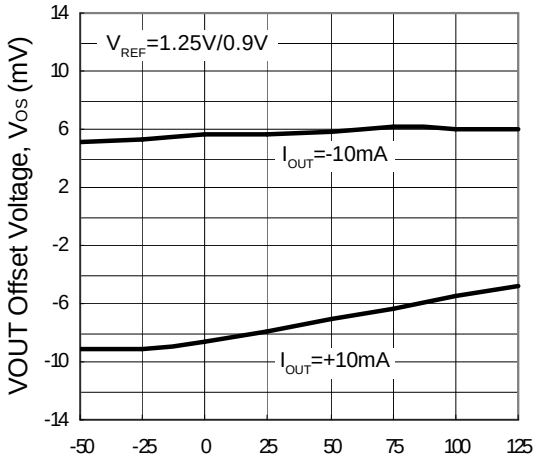


VREF Shutdown Threshold
vs Junction Temperature

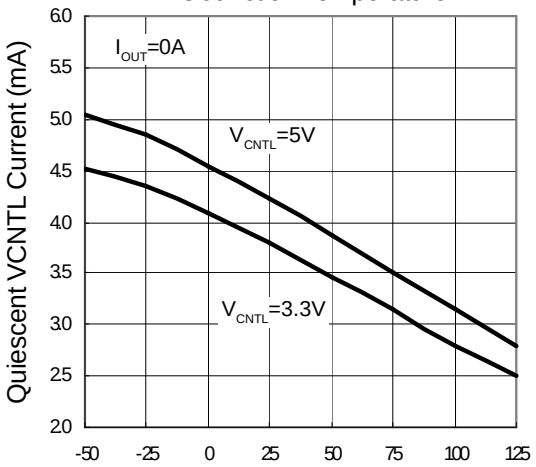


Typical Characteristics (Cont.)

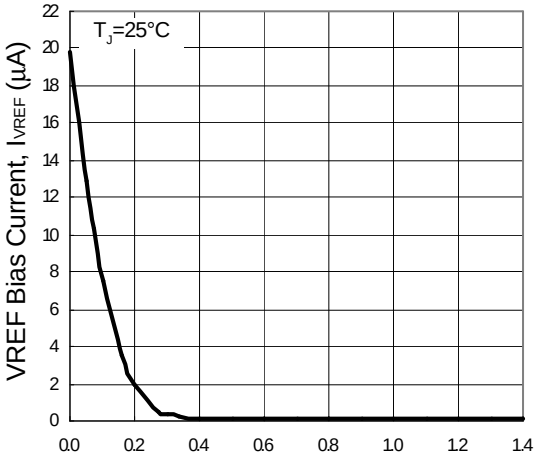
VOUT Offset Voltage
vs Junction Temperature



Quiescent VCNTL Current
vs Junction Temperature

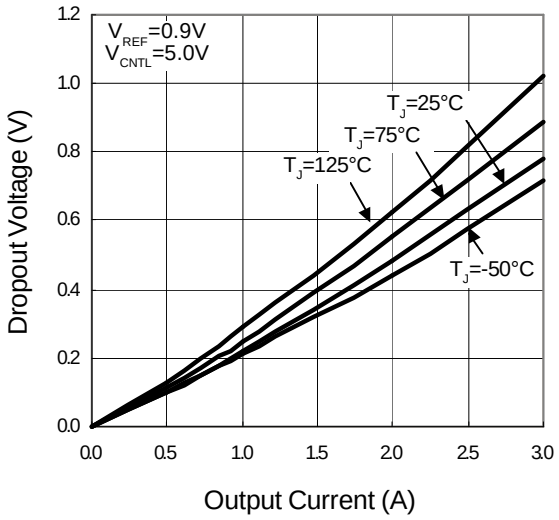


VREF Bias Current
vs VREF Supply Voltage

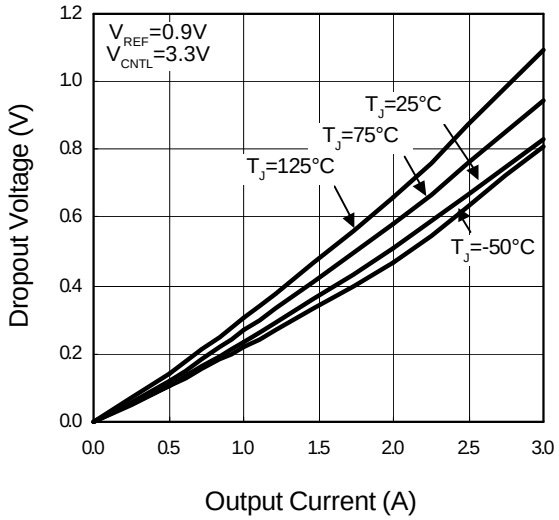


Typical Characteristics (Cont.)

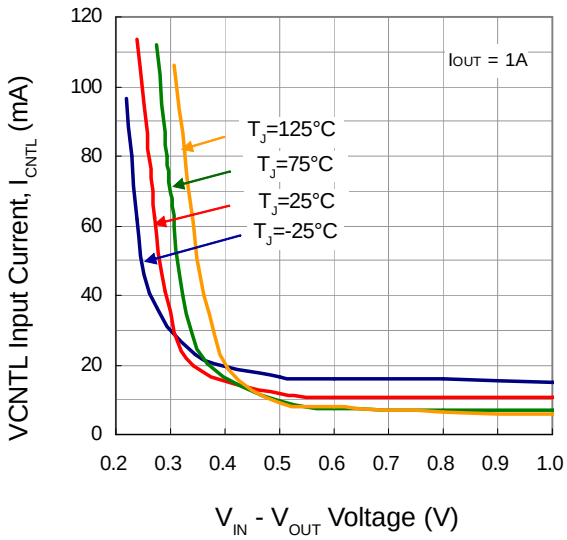
VIN Dropout Voltage vs. Output Current



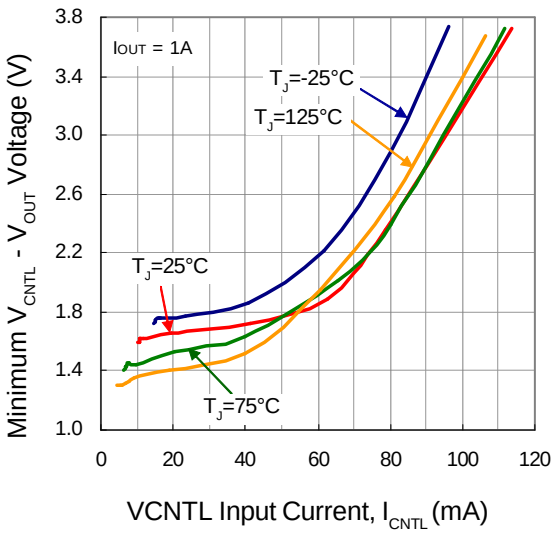
VIN Dropout Voltage vs. Output Current



VCNTL Input Current vs
V_{IN} - V_{OUT} Voltage at I_{OUT}=1A

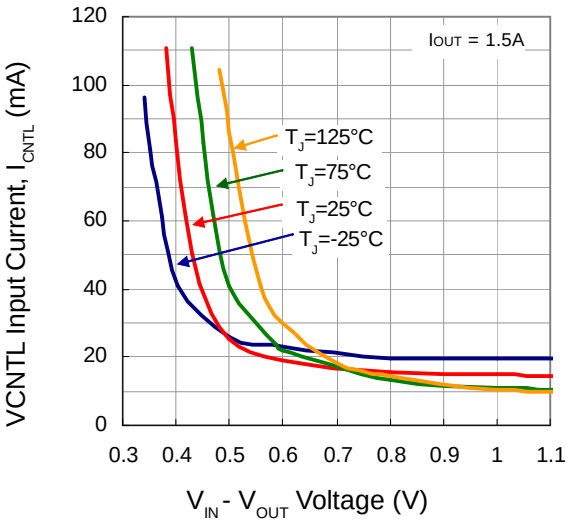


VCNTL-to-VOUT Dropout Voltage vs
VCNTL Input Current

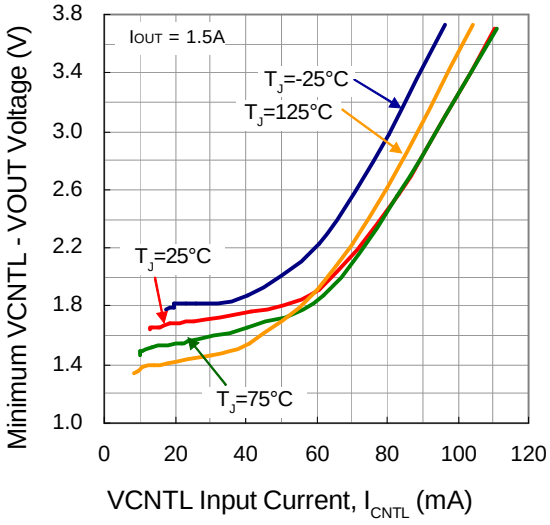


Typical Characteristics (Cont.)

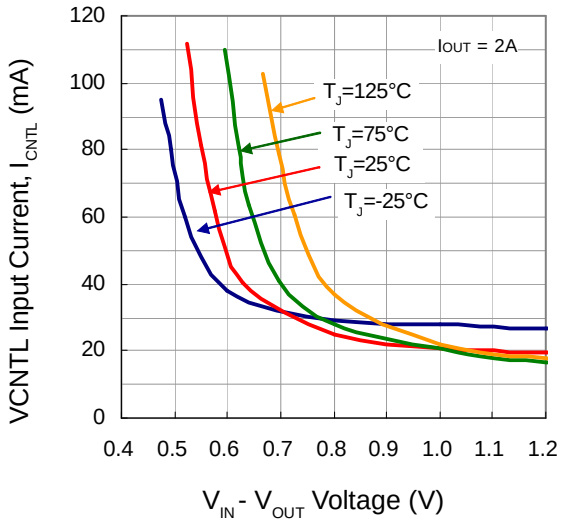
VCNTL Input Current vs
V_{IN} - V_{OUT} Voltage at I_{OUT}=1.5A



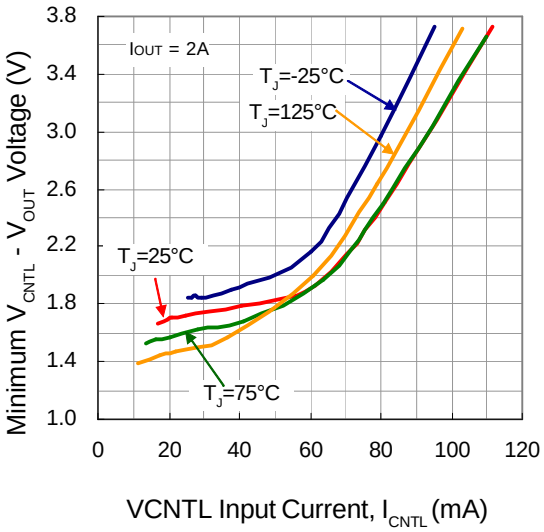
VCNTL-to-VOUT Dropout Voltage vs
VCNTL Input Current



VCNTL Input Current vs
V_{IN} - V_{OUT} Voltage at I_{OUT}=2A



VCNTL-to-VOUT Dropout Voltage vs
VCNTL Input Current

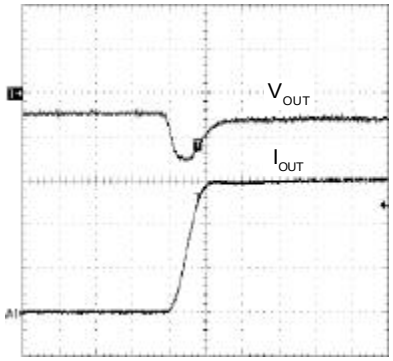


Operating Waveforms

1. Load Transient Response : I_{OUT} = +10mA -> +3A -> +10mA

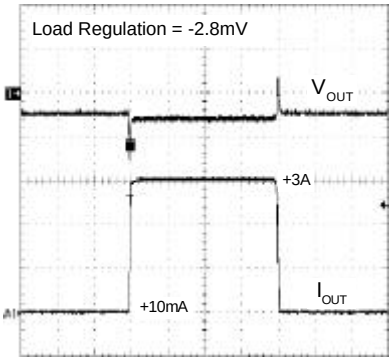
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = +10mA -> +3A



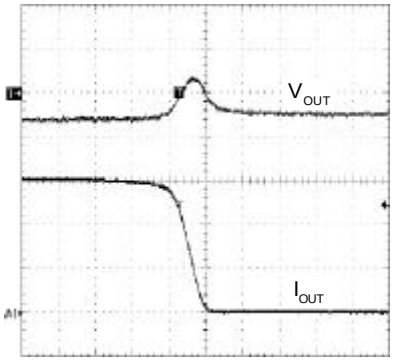
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

I_{OUT} = +10mA -> +3A -> +10mA



Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20µS/Div

I_{OUT} = +3A -> +10mA

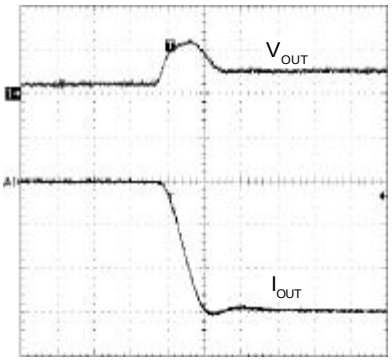


Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

2. Load Transient Response : I_{OUT} = -10mA -> -3A -> -10mA

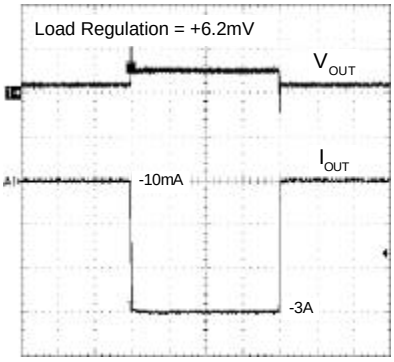
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = -10mA -> -3A



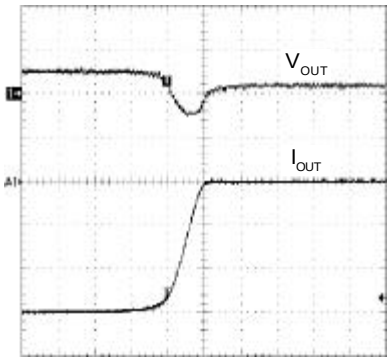
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

I_{OUT} = -10mA -> -3A -> -10mA



Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20µS/Div

I_{OUT} = -3A -> -10mA



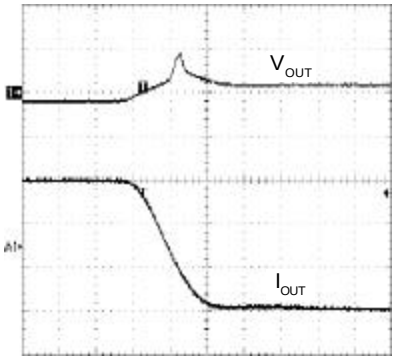
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

Operating Waveforms (Cont.)

3. Load Transient Response : I_{OUT} = +3A -> -3A -> +3A

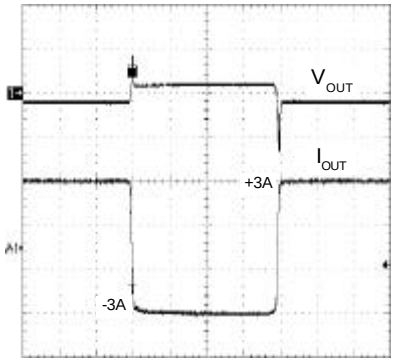
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = +3A -> -3A



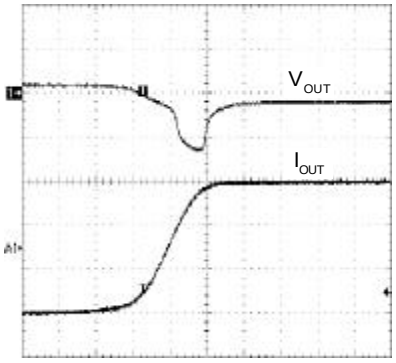
Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 1µS/Div

I_{OUT} = +3A -> -3A -> +3A



Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 20µS/Div

I_{OUT} = -3A -> +3A

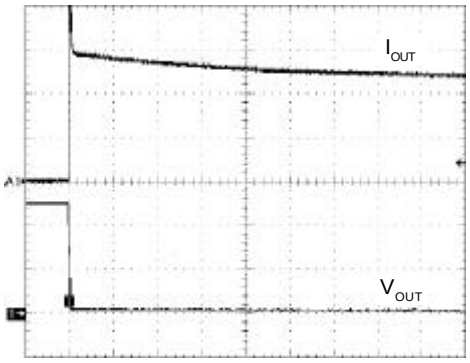


Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 1µS/Div

4. Short-Circuit Test

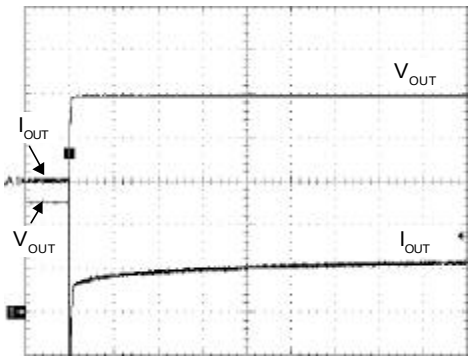
- V_{IN} = 2.5V, V_{CNTL} = 3.3V

V_{OUT} is Shorted to GND



Ch1 : V_{OUT}, 500mV/Div, DC,
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

V_{OUT} is Shorted to V_{IN} (2.5V)



Ch1 : V_{OUT}, 500mV/Div, DC,
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

Application Information

General

The APL5331 is a linear regulator and is capable of sourcing or sinking current up to 3A. The APL5331 has fast transient response, accurate output voltage (small voltage offset, load regulation), active-low shutdown control and fault protections (current-limit, thermal shutdown). The APL5331 is available in several packages to meet different of power dissipation in requirement various applications.

Output Voltage Regulation

The output voltage at VOUT pin tracks the reference voltage applied at VREF pin. Two internal NPN pass transistors controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN pin or sinking current to GND pin. The base currents of the pass transistors are provided by VCNTL pin. An internal kelvin sensing scheme senses the output voltage on VOUT pin for perfect load regulation. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. This results in higher output voltage while the regulator sinks load current. Since the APL5331 exhibits very fast load transient response, lesser amount of capacitors can be used. In addition, capacitors with high ESR can also be used.

Current Limit

The APL5331 monitors sourcing and sinking output currents, and limits the maximum output currents to prevent damages during overload or short-circuit condition. To increase the voltage across the internal pass transistors will get higher current-limit points.

Shutdown and Soft-Start

The VREF pin is a dual-function input pin, acting as reference input and shutdown control input. Applying

Shutdown and Soft-Start (Cont.)

and holding a voltage below 0.35V (typ.) to VREF pin shuts down the output of the regulator. An NPN transistor or N-channel MOSFET is used to pull down the VREF voltage while applying a “high” signal to turn on the transistor. When shutdown function is active, both pass transistors are turned off and the impedance of the VOUT is about 10MΩ (typ.), sourcing or sinking no current. When release the VREF pin, the current through the resistor divider charges the soft-start capacitor to initiate a soft-start process which controls the rise rate of the output voltage and limits the input surge current.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5331. When the junction temperature exceeds T_J= +183°C, a thermal sensor turns off both pass transistors, allowing the device to cool down. The regulator starts to regulate again after the junction temperature reduces by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit designed with a 40°C hysteresis lowers the average T_J during continuous thermal overload conditions, and extends life time of APL5331.

Power Inputs

It's not necessary to pay attention to the sequencing of the input voltages on VIN and VCNTL pins. However, do not apply a voltage to VOUT when the VCNTL voltage is not present. This reason is that the internal parasitic diodes connected from VOUT to VIN and from VOUT to VCNTL will be forward biased. When the VIN input voltage is not present, the APL5331 can only source few current up to 100mA to output. In the same condition, the APL5331 keeps same capability of sinking output current up to 3A.

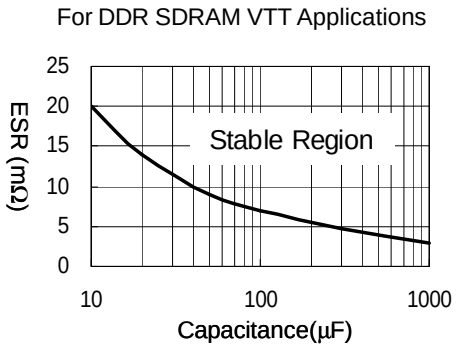
Application Information (Cont.)

Reference Voltage

A reference voltage is applied at the VREF pin by a resistor divider between VIN and GND pins. Normally, the bias current flowing out of the VREF pin and is about 150nA (typ.), creating voltage offset at the resistor divider and affecting the output voltage accuracy. The recommended resistor is <5kΩ to maintain accuracy of the output voltage. An external bypass capacitor (>0.1uF) is also connected to VREF. The capacitor and the resistor divider form a low-pass filter to reduce the inherent reference noise from VIN. Connect the capacitor as close to VREF as possible for optimal effect. Do not place any additional loading on this reference input pin.

Output Capacitor

The APL5331 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon the ESR (equivalent series resistance) and capacitance of the output capacitor over full temperature range. The following chart shows the stable region of the output capacitor for APL5331. The stable region is above the curve, indicating minimum required ESR and capacitance to maintain stability. However, the output capacitor should have an ESR less than 1Ω.



Output Capacitor (Cont.)

Ultra-low-ESR capacitors, such as ceramic chip capacitors, may promote under-damped transient

response, but proper ceramic chip capacitors placed near loads can be used as decoupling capacitors. A low-ESR solid tantalum and aluminum electrolytic capacitor (ESR<1Ω) works extremely well and provides good transient response and stability over temperature.

The output capacitors are also used to reduce the slew rate of load current and help the APL5331 to minimize variations of the output voltage, improving transient response. For this purpose, the low-ESR capacitors depending on the step size and slew rate of a load current step are recommended.

Input Capacitor

The input capacitors for VCNTL and VIN pins are not required for stability but for supplying surge currents during large load transients. The input capacitors prevent the input rail from dipping to improve the performance of the APL5331. Reducing the parasitic inductance and resistance of current paths from power sources to the APL5331 also reduces voltage dips on VCNTL and VIN pins.

A capacitor of 1μF (ceramic chip capacitor) or greater (aluminum electrolytic capacitor) is recommended for VCNTL pin. For VIN pin, an aluminum electrolytic capacitor (>50μF) is recommended. It is not necessary to use low-ESR capacitors.

Layout and Thermal Consideration

The input capacitors for VIN and VCNTL pins are normally placed near each pin for good performances. Ceramic decoupling capacitors for loads must be placed as close to the loads to reduce the parasitic inductors of traces. It is also recommended that the APL5331 and output capacitors are placed near the load for good load

Application Information (Cont.)

regulation and load transient response. The negative pins of the input and output capacitors and the GND pin of the APL5331 should connect to analog ground plane of the load.

See figure 1. The SOP-8-P utilizes a bottom thermal pad to minimize the thermal resistance of the package, making the package suitable for high current applications. The thermal pad is soldered to the top ground pad and is connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into the ambient air. The vias are recommended to have proper size to retain solder, helping heat conduction.

Thermal resistance consists of two main elements, θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). θ_{JC} is specified from the IC junction to the bottom of the thermal pad directly below the die. θ_{CA} is the resistance from the bottom of thermal pad to the ambient air and it includes θ_{CS} (case-to-sink thermal resistance) and θ_{SA} (sink-to-ambient thermal resistance). The specified path for heat flow is the lowest resistance path and it dissipates majority of the heat to the ambient air. Typically, θ_{CA} is the dominant thermal resistance. Therefore, enlarging the internal or bottom ground plane reduces the resistance θ_{CA}. The relationship between power dissipation and temperatures is the following equation:

$$P_D = (T_J - T_A) / \leq \theta_{JA}$$

where,

P_D : Power dissipation

T_J : Junction Temperature

T_A : Ambient Temperature

θ_{JA}: Junction-to-Ambient Thermal Resistance

Figure 2 shows a board layout using the SOP-8-P package. The demo board is made of FR-4 material

Layout and Thermal Consideration (Cont.)

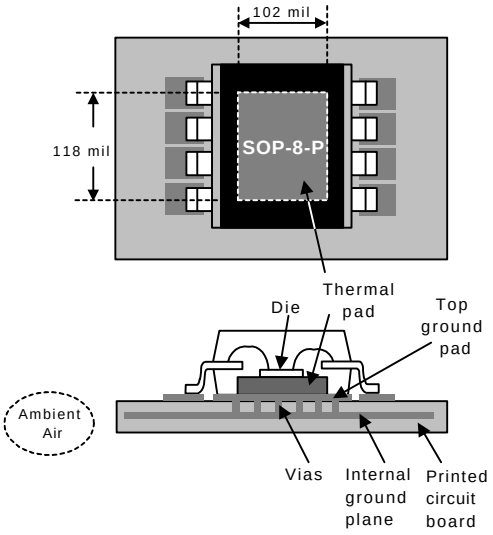


Figure 1 Package Top and side view

and is a two-layer PCB. The size and thickness are 65mm* 65mm and 1.6mm. An area of 140mil*105mil on the top layer is use as a thermal pad for the APL5331 and this is connected to the bottom layer by vias. The bottom layer using 2 oz. copper acts as the ground plane for the system. The PCB and all components on the board form a heat sink. The θ_{JA} of the APL5331 (SOP-8-P) mounted on this demo board is about 37°C/W in free air. Assuming the T_A=25°C and the maximum T_J = 150°C (typical thermal limit temperature), the maximum power dissipation is calculated as :

$$P_D(max) = (150 - 25) / 37$$
$$= 3.38W$$

If the T_J is designed to be below 125°C, the calculated power dissipation should be less than :

$$P_D = (125 - 25) / 37$$
$$= 2.70W$$

Application Information (Cont.)

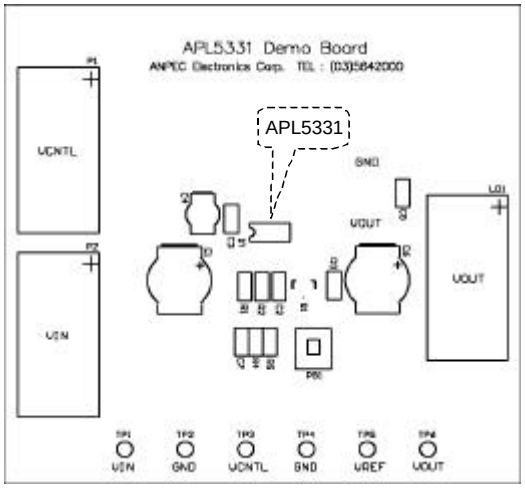


Figure 2(a) TopOver layer

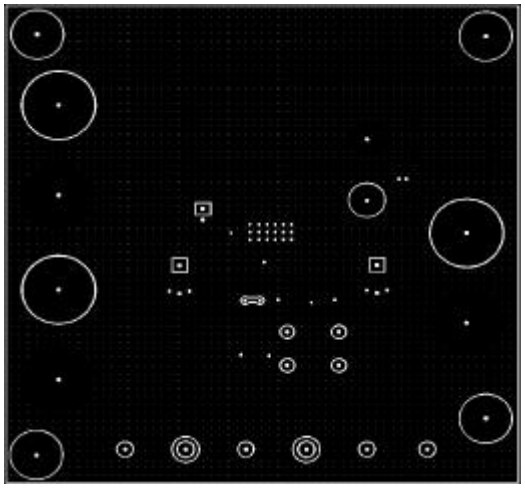


Figure 2(c) Bottom layer

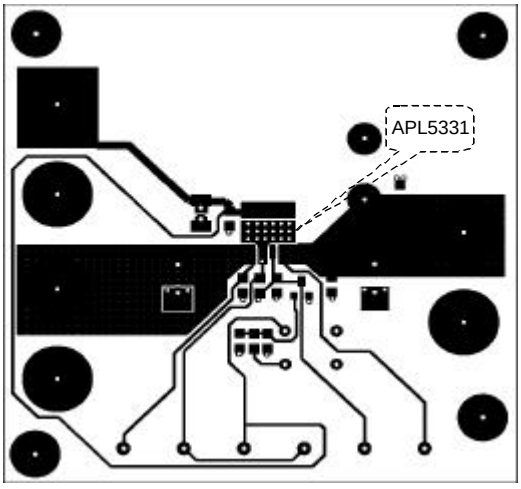
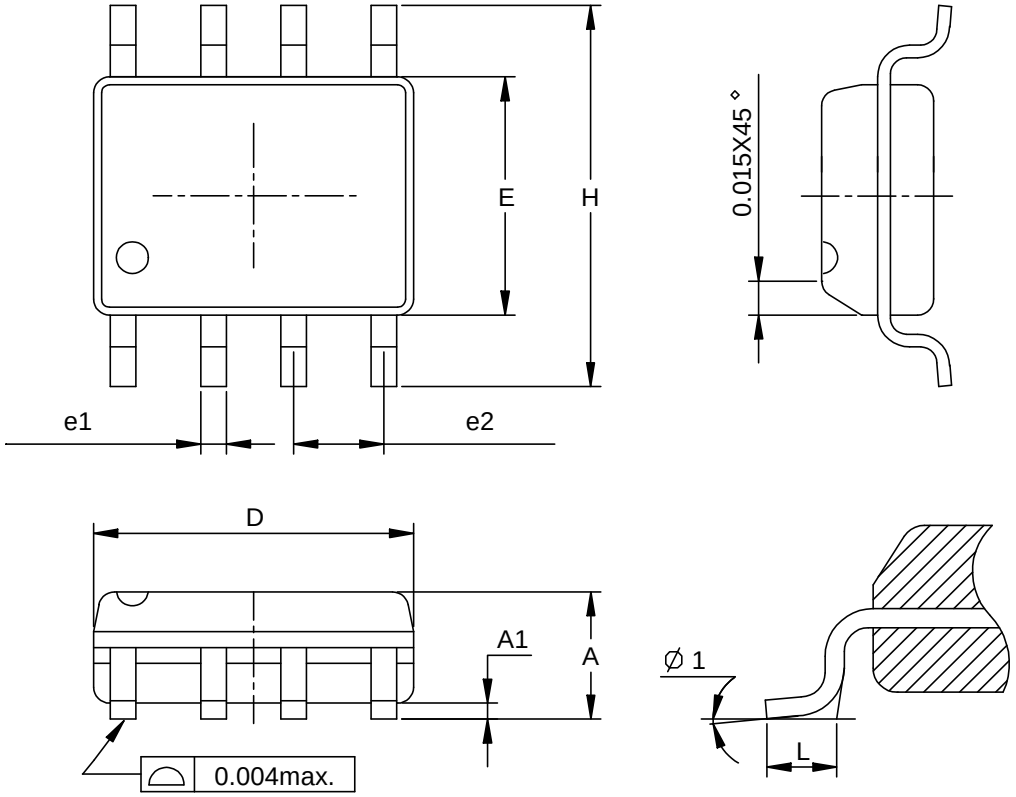


Figure 2(b) Top layer

Packaging Information

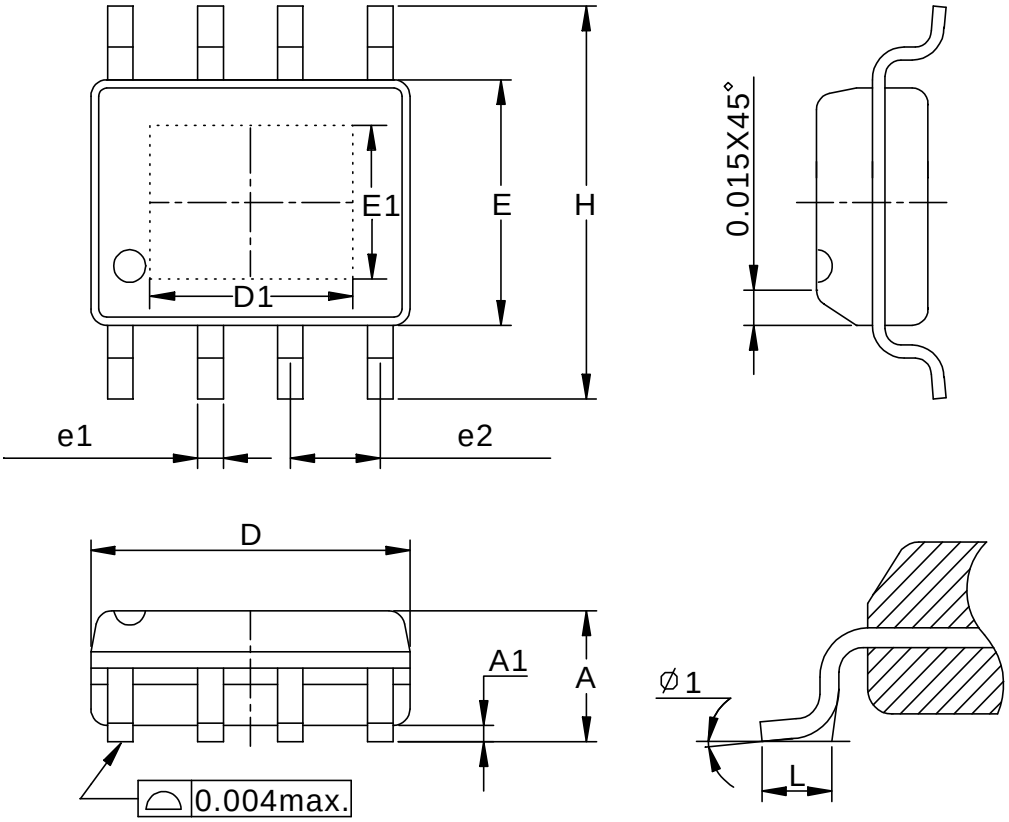
SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	0°	8°	0°	8°

Packaging Information

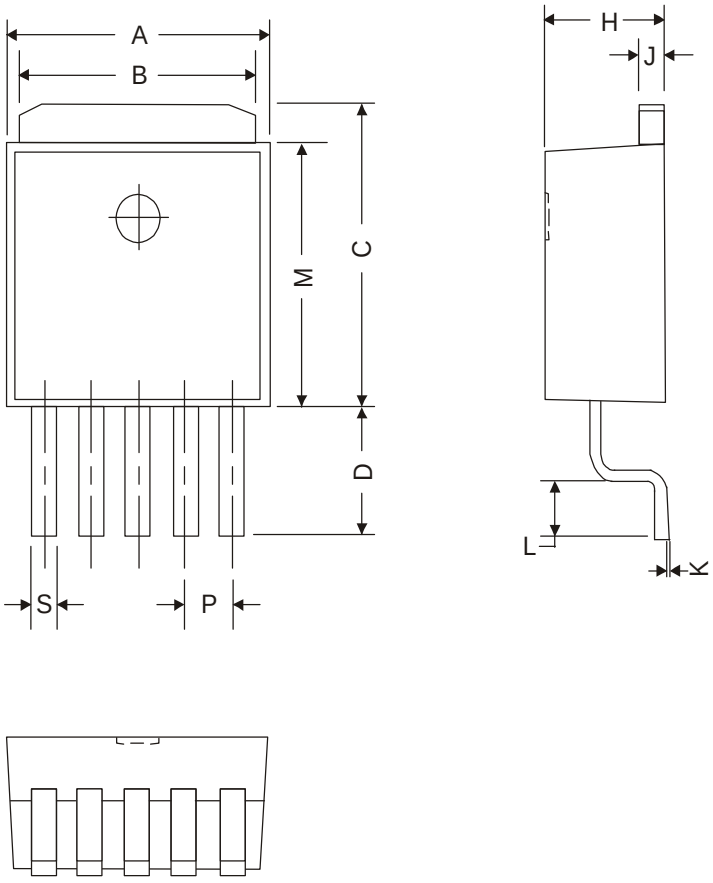
SOP-8-P pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Packaging Information

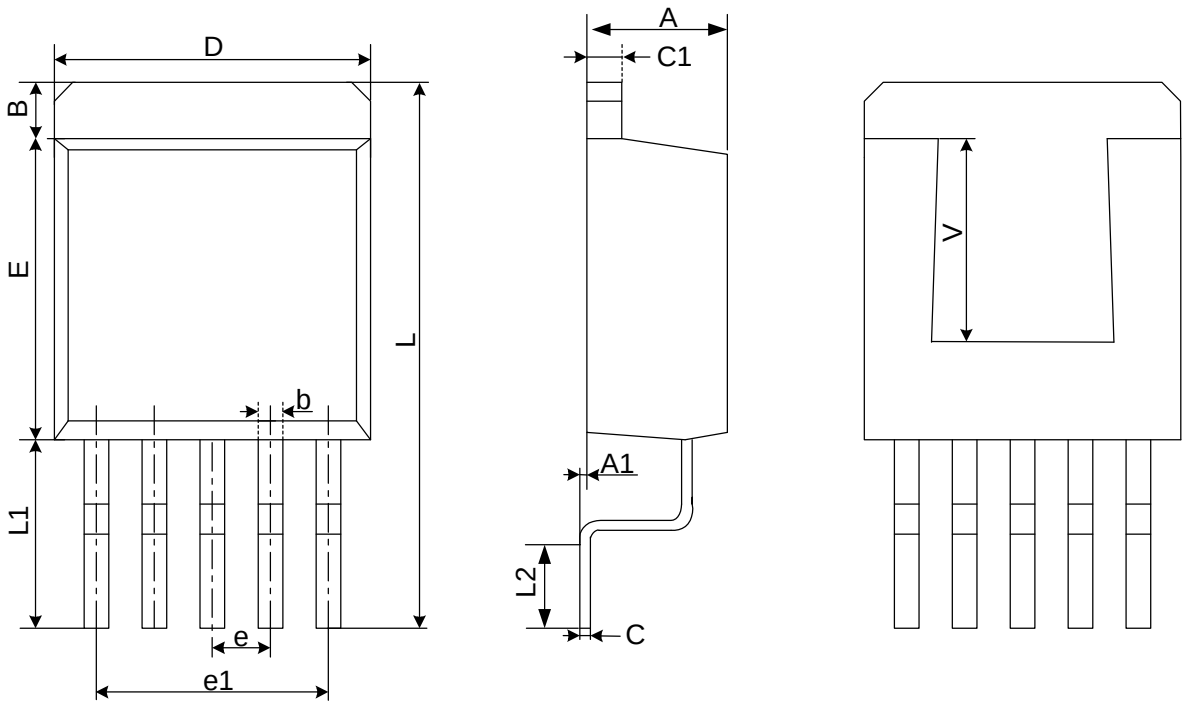
TO-252-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	6.40	6.80	0.25	0.26
B	5.20	5.50	0.20	0.21
C	6.80	7.20	0.26	0.27
D	2.20	2.80	0.08	0.11
P	1.27 REF		0.05 REF	
S	0.50	0.80	0.02	0.03
H	2.20	2.40	0.08	0.09
J	0.45	0.55	0.01	0.02
K	0	0.15	0	0.006
L	0.90	1.50	0.03	0.06
M	5.40	5.80	0.21	0.22

Package Information

TO-263-5

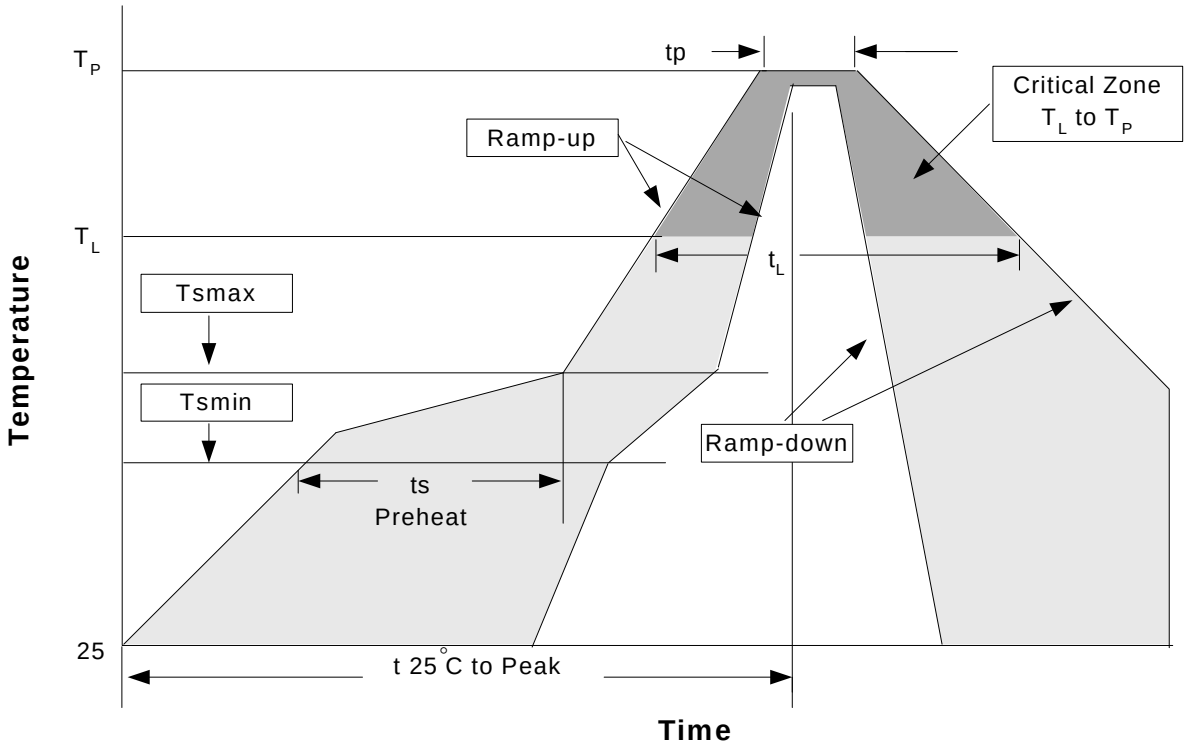


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.06	4.83	0.160	0.190
A1	0.00	0.15	0.000	0.006
B	1.40	1.76	0.055	0.069
b	0.50	0.99	0.020	0.039
C	0.310	0.736	0.012	0.029
C1	1.14	1.40	0.045	0.055
D	9.65	10.29	0.380	0.405
E	8.20	9.66	0.323	0.380
e	1.52	1.83	0.060	0.072
e1	6.70	6.90	0.264	0.272
L	14.60	15.88	0.575	0.625
L1	5.08	5.48	0.200	0.216
L2	2.28	2.80	0.090	0.110
V	5.600REF		0.220REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

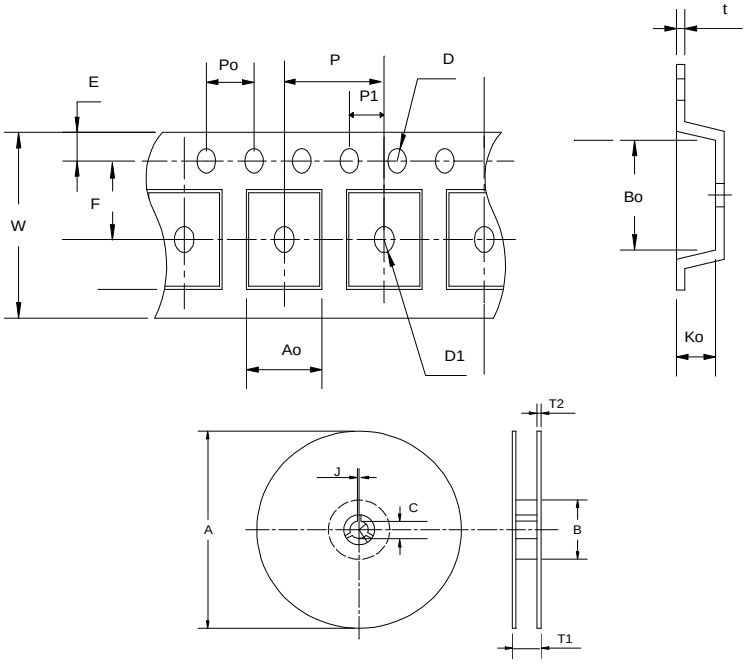
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape



Carrier Tape(Cont.)

Application	A	B	C	J	T1	T2	W	P	E
SOP- 8 SOP-8-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013
Application	A	B	C	J	T1	T2	W	P	E
TO-252	330 ±3	100 ± 2	13 ± 0. 5	2 ± 0.5	16.4 + 0.3 -0.2	2.5± 0.5	16+ 0.3 - 0.1	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.8 ± 0.1	10.4± 0.1	2.5± 0.1	0.3±0.05
Application	A	B	C	J	T1	T2	W	P	E
TO-263	380±3	80 ± 2	13 ± 0. 5	2 ± 0.5	24 ± 4	2± 0.3	24 + 0.3 - 0.1	16 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	10.8 ± 0.1	16.1± 0.1	5.2± 0.1	0.35±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8 / SOP-8-P	12	9.3	2500
TO- 252	16	13.3	2500
TO- 263	24	21.3	1000

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