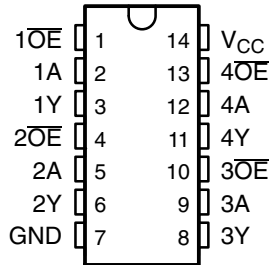


# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

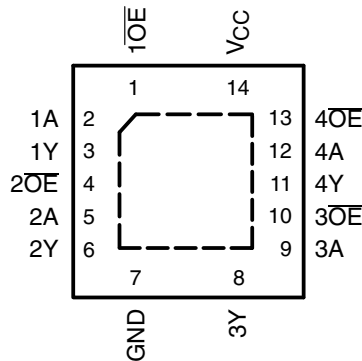
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- Typical  $V_{OLP}$  (Output Ground Bounce)  $<1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

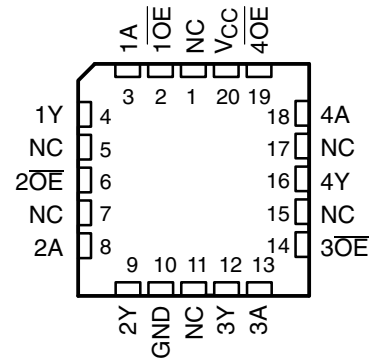
SN54ABT125 . . . J OR W PACKAGE  
SN74ABT125 . . . D, DB, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74ABT125 . . . RGY PACKAGE  
(TOP VIEW)



SN54ABT125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'ABT125 quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$                                     | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------------------------------------|------------|---------------|-----------------------|------------------|
| $-40^\circ\text{C to } 85^\circ\text{C}$  | PDIP – N   | Tube          | SN74ABT125N           | SN74ABT125N      |
|                                           | QFN – RGY  | Tape and reel | SN74ABT125RGYR        | AB125            |
|                                           | SOIC – D   | Tube          | SN74ABT125D           | ABT125           |
|                                           |            | Tape and reel | SN74ABT125DR          |                  |
|                                           | SOP – NS   | Tape and reel | SN74ABT125NSR         | ABT125           |
|                                           | SSOP – DB  | Tape and reel | SN74ABT125DBR         | AB125            |
|                                           | TSSOP – PW | Tape and reel | SN74ABT125PWR         | AB125            |
| $-55^\circ\text{C to } 125^\circ\text{C}$ | CDIP – J   | Tube          | SNJ54ABT125J          | SNJ54ABT125J     |
|                                           | CFP – W    | Tube          | SNJ54ABT125W          | SNJ54ABT125W     |
|                                           | LCCC – FK  | Tube          | SNJ54ABT125FK         | SNJ54ABT125FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABT125, SN74ABT125

## QUADRUPLE BUS BUFFER GATES

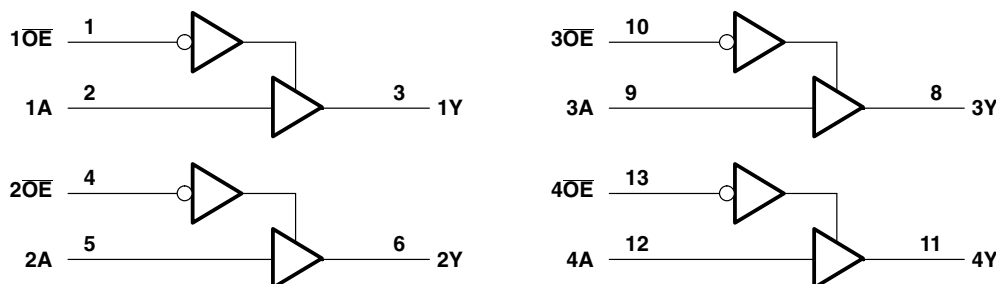
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| OE     | A | Y      |
| L      | H | H      |
| L      | L | L      |
| H      | X | Z      |

#### logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, RGY, and W packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT125              | 96 mA           |
| SN74ABT125                                                                | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package          | 86°C/W          |
| (see Note 2): DB package                                                  | 96°C/W          |
| (see Note 2): N package                                                   | 80°C/W          |
| (see Note 2): NS package                                                  | 76°C/W          |
| (see Note 2): PW package                                                  | 113°C/W         |
| (see Note 3): RGY package                                                 | 47°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. The package thermal impedance is calculated in accordance with JESD 51-7.
  3. The package thermal impedance is calculated in accordance with JESD 51-5.



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# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 4)

|                          |                                    | SN54ABT125 |          | SN74ABT125 |          | UNIT      |
|--------------------------|------------------------------------|------------|----------|------------|----------|-----------|
|                          |                                    | MIN        | MAX      | MIN        | MAX      |           |
| $V_{CC}$                 | Supply voltage                     | 4.5        | 5.5      | 4.5        | 5.5      | V         |
| $V_{IH}$                 | High-level input voltage           | 2          |          | 2          |          | V         |
| $V_{IL}$                 | Low-level input voltage            |            | 0.8      |            | 0.8      | V         |
| $V_I$                    | Input voltage                      | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V         |
| $I_{OH}$                 | High-level output current          |            | –24      |            | –32      | mA        |
| $I_{OL}$                 | Low-level output current           |            | 48       |            | 64       | mA        |
| $\Delta t/\Delta v$      | Input transition rise or fall rate |            | 10       |            | 10       | ns/V      |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200        |          | 200        |          | $\mu$ s/V |
| $T_A$                    | Operating free-air temperature     | –55        | 125      | –40        | 85       | °C        |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ABT125, SN74ABT125

## QUADRUPLE BUS BUFFER GATES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | TEST CONDITIONS                                                                      |                                                                                     | T <sub>A</sub> = 25°C |      |       | SN54ABT125 |       | SN74ABT125 |       | UNIT |
|--------------------|--------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------------------|------|-------|------------|-------|------------|-------|------|
|                    |                                                                                      |                                                                                     | MIN                   | TYP† | MAX   | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>IK</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                     |                                                                                     |                       |      | -1.2  |            | -1.2  |            | -1.2  | V    |
| V <sub>OH</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                     |                                                                                     | 2.5                   |      |       | 2.5        |       | 2.5        |       | V    |
|                    | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       |                                                                                     | 3                     |      |       | 3          |       | 3          |       |      |
|                    | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OH</sub> = -24 mA                                                            | 2                     |      |       | 2          |       |            |       |      |
|                    |                                                                                      | I <sub>OH</sub> = -32 mA                                                            | 2*                    |      |       |            |       | 2          |       |      |
| V <sub>OL</sub>    | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OL</sub> = 48 mA                                                             |                       |      | 0.55  |            | 0.55  |            |       | V    |
|                    |                                                                                      | I <sub>OL</sub> = 64 mA                                                             |                       |      | 0.55* |            |       |            | 0.55  |      |
| V <sub>hys</sub>   |                                                                                      |                                                                                     |                       | 100  |       |            |       |            |       | mV   |
| I <sub>I</sub>     | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                |                                                                                     |                       |      | ±1    |            | ±1    |            | ±1    | μA   |
| I <sub>OZPU</sub>  | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                                                                                     |                       |      | ±50   |            | ±50   |            | ±50   | μA   |
| I <sub>OZPD</sub>  | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                                                                                     |                       |      | ±50   |            | ±50   |            | ±50   | μA   |
| I <sub>OZH</sub>   | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V   |                                                                                     |                       |      | 10    |            | 10    |            | 10    | μA   |
| I <sub>OZL</sub>   | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V   |                                                                                     |                       |      | -10   |            | -10   |            | -10   | μA   |
| I <sub>off</sub>   | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                                                                                     |                       |      | ±100  |            |       |            | ±100  | μA   |
| I <sub>CEX</sub>   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      | Outputs high                                                                        |                       |      | 50    |            | 50    |            | 50    | μA   |
| I <sub>O‡</sub>    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      |                                                                                     | -50                   | -100 | -200§ | -50        | -200§ | -50        | -200§ | mA   |
| I <sub>CC</sub>    | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high                                                                        |                       | 1    | 250   |            | 250   |            | 250   | μA   |
|                    |                                                                                      | Outputs low                                                                         |                       | 24   | 30    |            | 30    |            | 30    | mA   |
|                    |                                                                                      | Outputs disabled                                                                    |                       | 0.5  | 250   |            | 250   |            | 250   | μA   |
| ΔI <sub>CC</sub> ¶ | Data inputs                                                                          | One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND                          |                       |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
|                    |                                                                                      | Outputs disabled                                                                    |                       |      | 0.05  |            | 0.05  |            | 0.05  |      |
|                    | Control inputs                                                                       | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND |                       |      | 1.5   |            | 1.5   |            | 1.5   |      |
| C <sub>i</sub>     | V <sub>I</sub> = 2.5 V or 0.5 V                                                      |                                                                                     |                       | 3    |       |            |       |            |       | pF   |
| C <sub>o</sub>     | V <sub>O</sub> = 2.5 V or 0.5 V                                                      |                                                                                     |                       | 7    |       |            |       |            |       | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This limit may vary among suppliers.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.



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# **SN54ABT125, SN74ABT125** **QUADRUPLE BUS BUFFER GATES** **WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

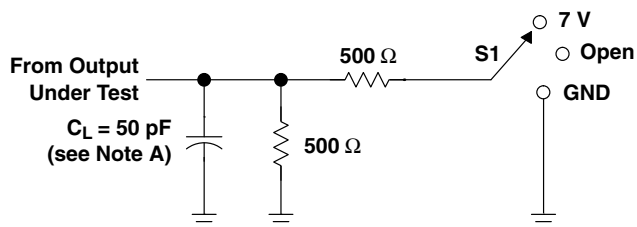
| PARAMETER         | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5\text{ V},$<br>$T_A = 25^\circ\text{C}$ |     |     | SN54ABT125 |     | SN74ABT125 |     | UNIT |
|-------------------|-----------------|----------------|----------------------------------------------------|-----|-----|------------|-----|------------|-----|------|
|                   |                 |                | MIN                                                | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{PLH}^\dagger$ | A               | Y              | 1                                                  | 3.2 | 4.6 | 1          | 6   | 1          | 4.9 | ns   |
| $t_{PHL}^\dagger$ |                 |                | 1                                                  | 2.5 | 4.6 | 1          | 6.2 | 1          | 4.9 |      |
| $t_{PZH}^\dagger$ | $\overline{OE}$ | Y              | 1                                                  | 3.6 | 5   | 1          | 6   | 1          | 5.9 | ns   |
| $t_{PZL}^\dagger$ |                 |                | 1                                                  | 2.5 | 6.2 | 1          | 7.5 | 1          | 6.8 |      |
| $t_{PHZ}$         | $\overline{OE}$ | Y              | 1                                                  | 3.8 | 5.4 | 1          | 6.3 | 1          | 6.2 | ns   |
| $t_{PLZ}^\dagger$ |                 |                | 1                                                  | 3.3 | 5.3 | 1          | 6.5 | 1          | 6.2 |      |

<sup>†</sup> This limit may vary among suppliers.

# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

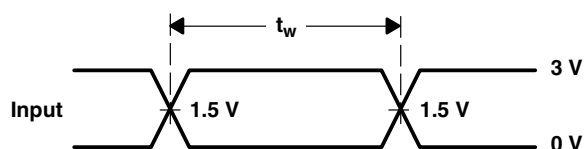
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## PARAMETER MEASUREMENT INFORMATION

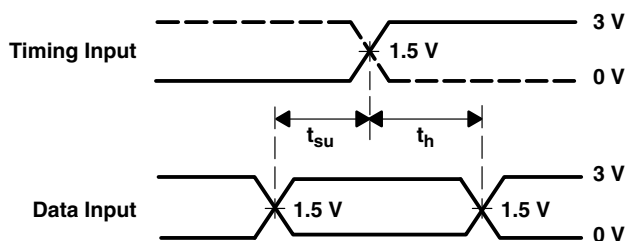


LOAD CIRCUIT

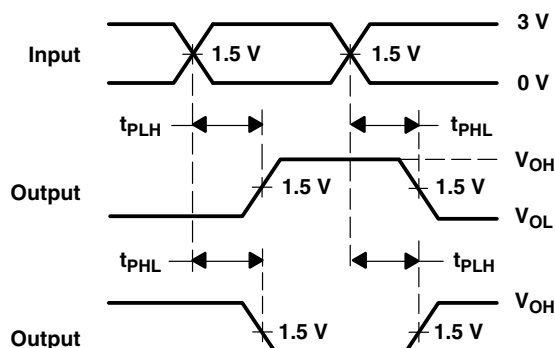
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



VOLTAGE WAVEFORMS  
PULSE DURATION



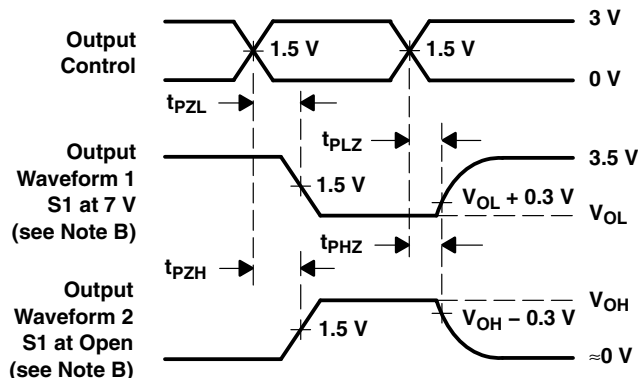
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

### INVERTING AND NONINVERTING OUTPUTS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - All parameters and waveforms are not applicable to all devices.



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|------------------------------------------|-------------------------|
| 5962-9676801Q2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9676801Q2A<br>SNJ54ABT<br>125FK | <a href="#">Samples</a> |
| 5962-9676801QCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9676801QC<br>A<br>SNJ54ABT125J      | <a href="#">Samples</a> |
| 5962-9676801QDA  | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9676801QD<br>A<br>SNJ54ABT125W      | <a href="#">Samples</a> |
| SN74ABT125D      | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125DBR    | ACTIVE        | SSOP         | DB                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                                    | <a href="#">Samples</a> |
| SN74ABT125DE4    | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125DG4    | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125DR     | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125DRE4   | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125DRG4   | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125N      | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | SN74ABT125N                              | <a href="#">Samples</a> |
| SN74ABT125NSR    | ACTIVE        | SO           | NS                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT125                                   | <a href="#">Samples</a> |
| SN74ABT125PW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                                    | <a href="#">Samples</a> |
| SN74ABT125PWG4   | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                                    | <a href="#">Samples</a> |
| SN74ABT125PWR    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)             | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74ABT125PWRE4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                               | <a href="#">Samples</a> |
| SN74ABT125PWRG4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB125                               | <a href="#">Samples</a> |
| SN74ABT125RGYR   | ACTIVE        | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | AB125                               | <a href="#">Samples</a> |
| SNJ54ABT125FK    | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-9676801Q2A<br>SNJ54ABT125FK    | <a href="#">Samples</a> |
| SNJ54ABT125J     | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9676801QC<br>A<br>SNJ54ABT125J | <a href="#">Samples</a> |
| SNJ54ABT125W     | ACTIVE        | CFP          | W               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9676801QD<br>A<br>SNJ54ABT125W | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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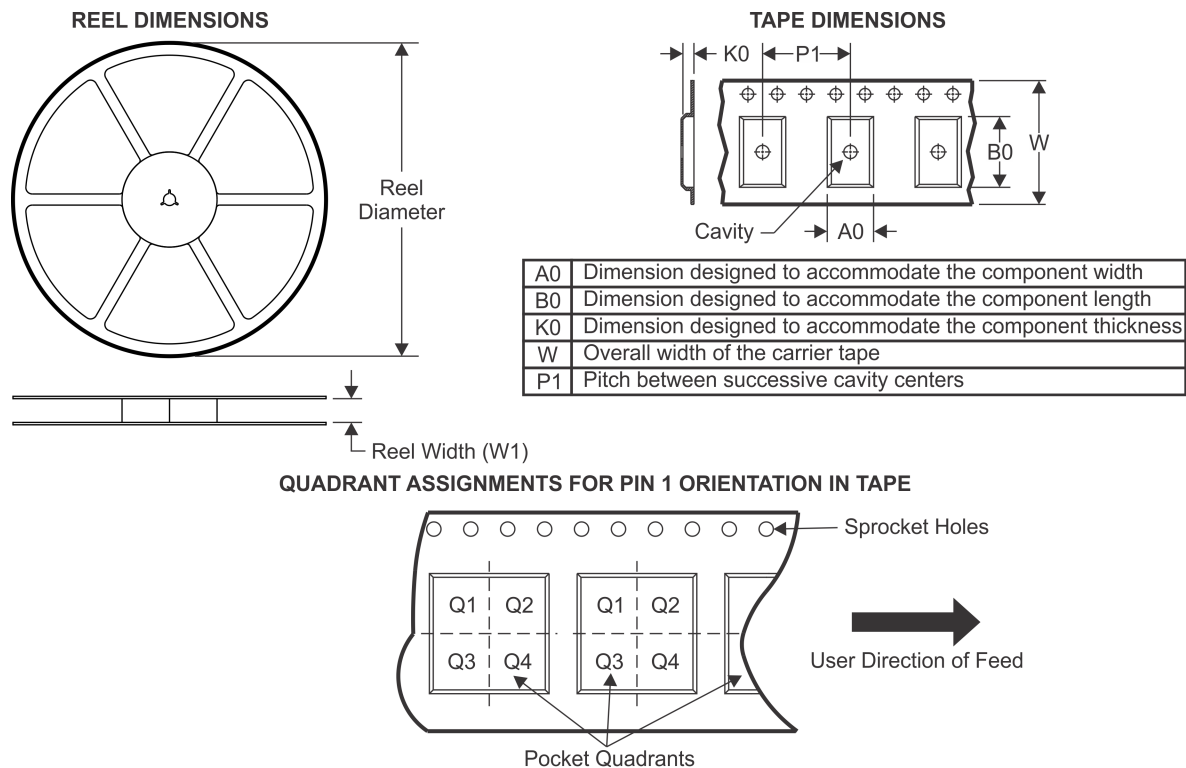
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ABT125, SN74ABT125 :**

- Catalog: [SN74ABT125](#)
- Military: [SN54ABT125](#)

NOTE: Qualified Version Definitions:

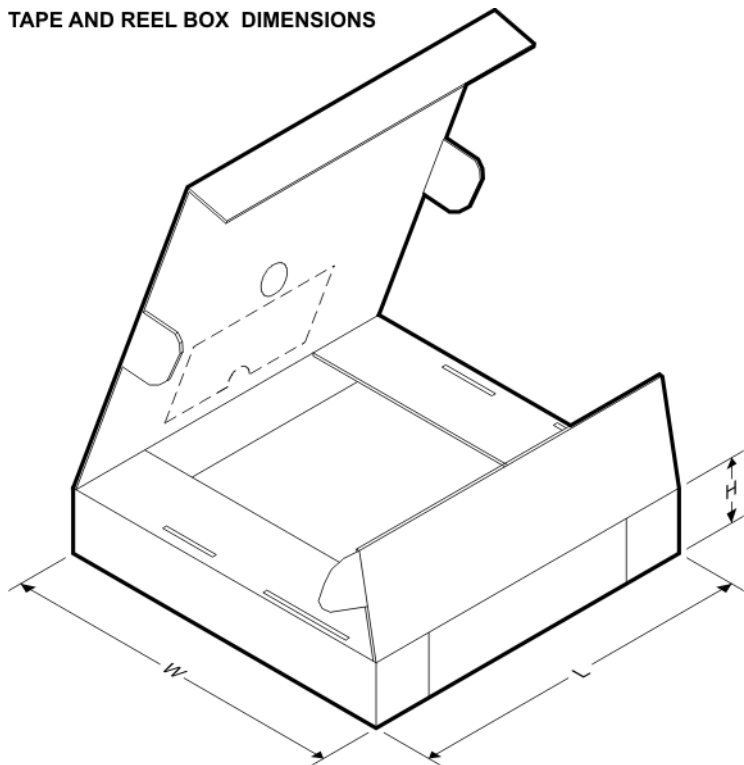
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT125DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ABT125DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ABT125NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT125PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ABT125RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



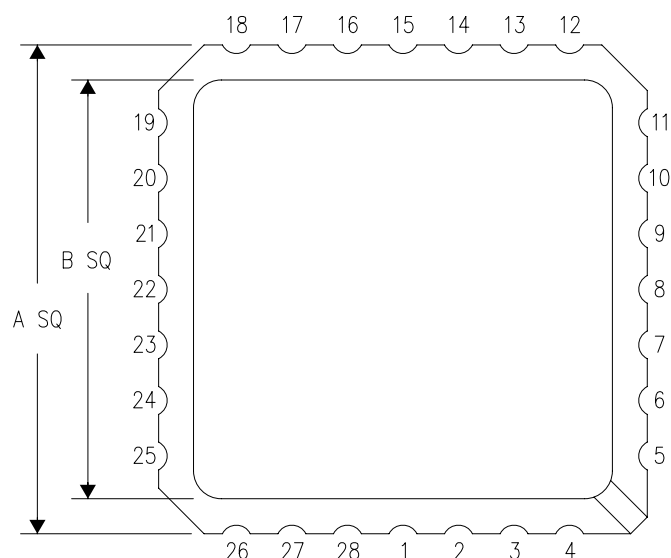
\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT125DR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74ABT125DR   | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74ABT125NSR  | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74ABT125PWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74ABT125RGYR | VQFN         | RGY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |

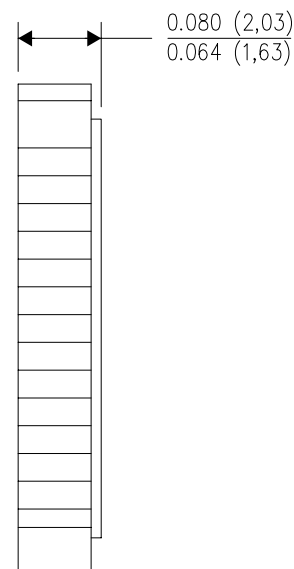
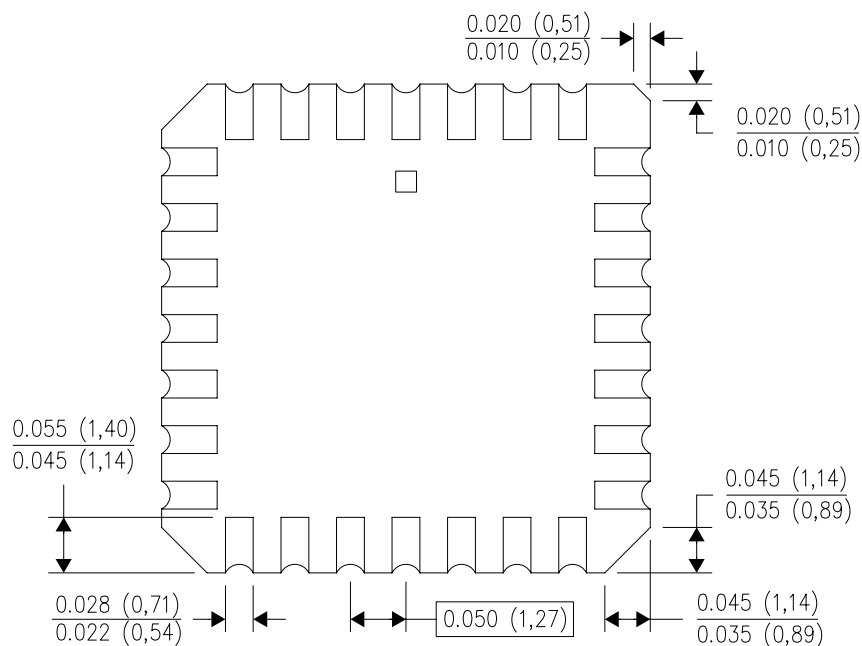
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |

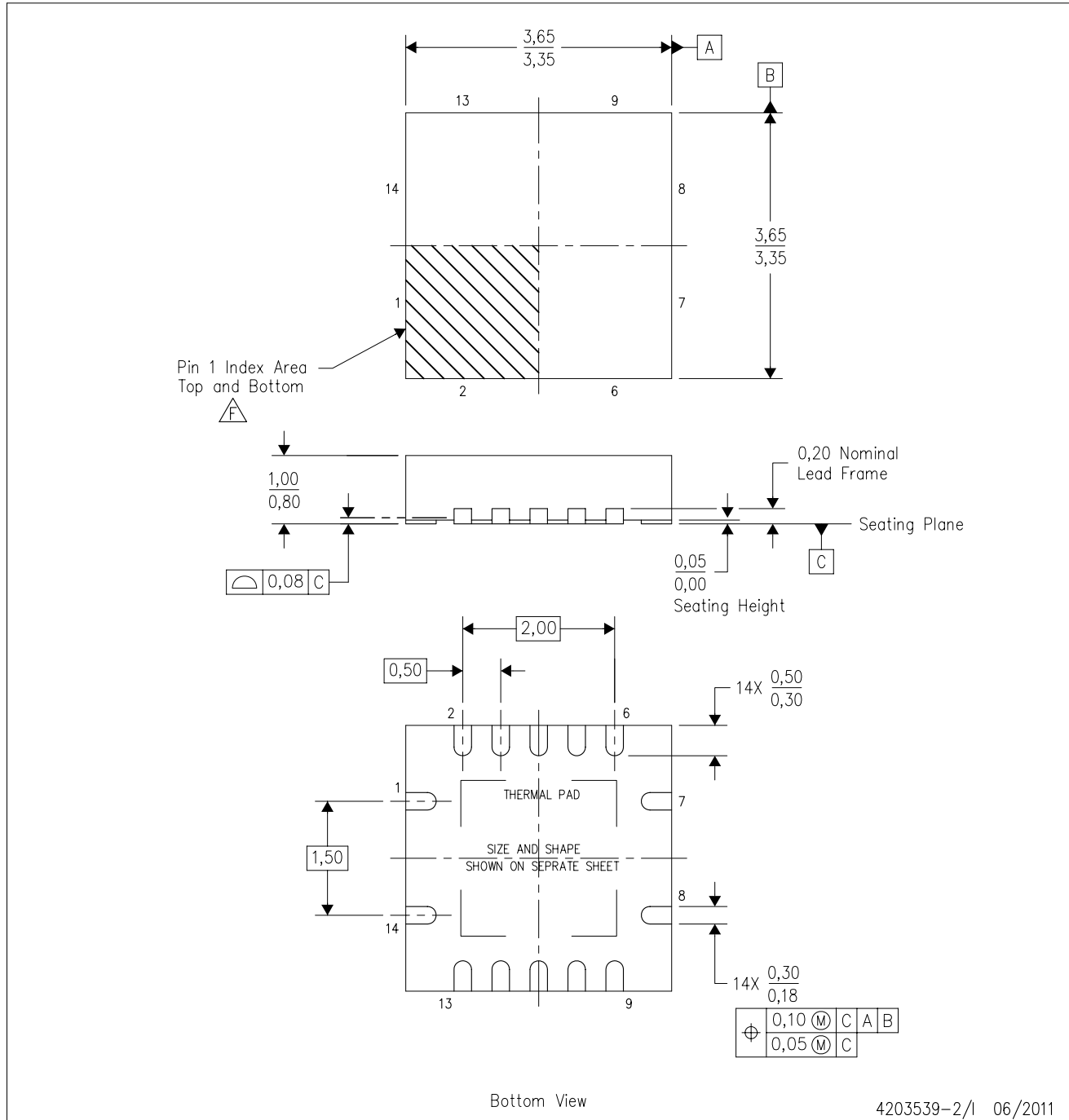


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

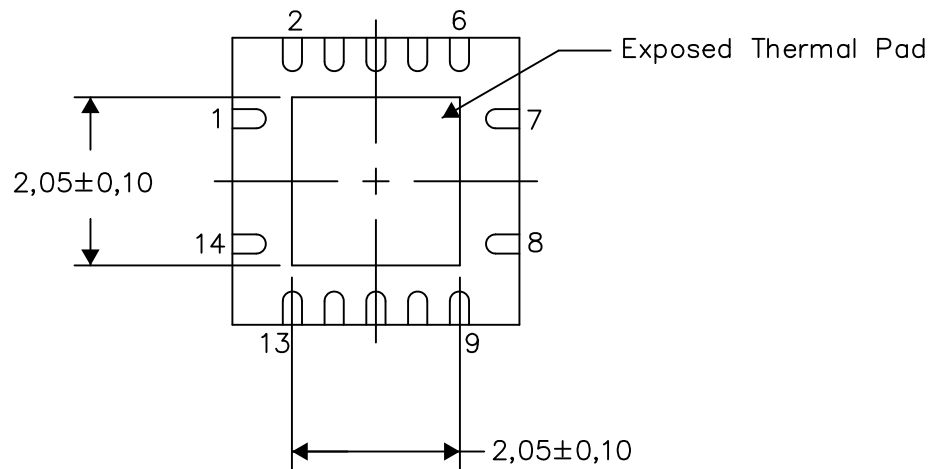
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

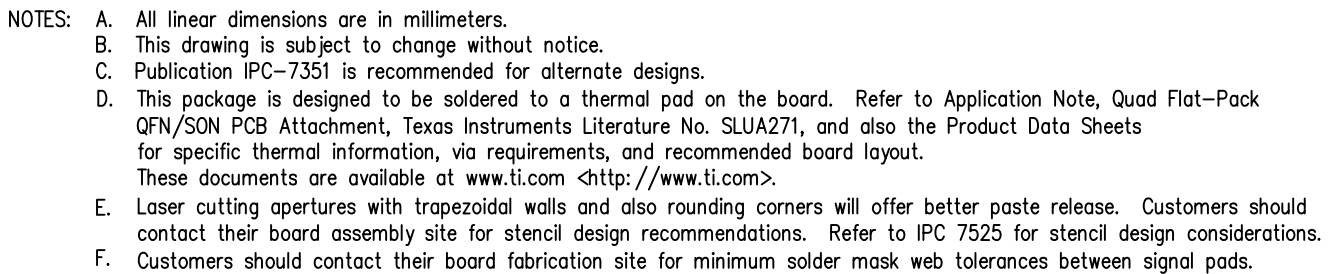


Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

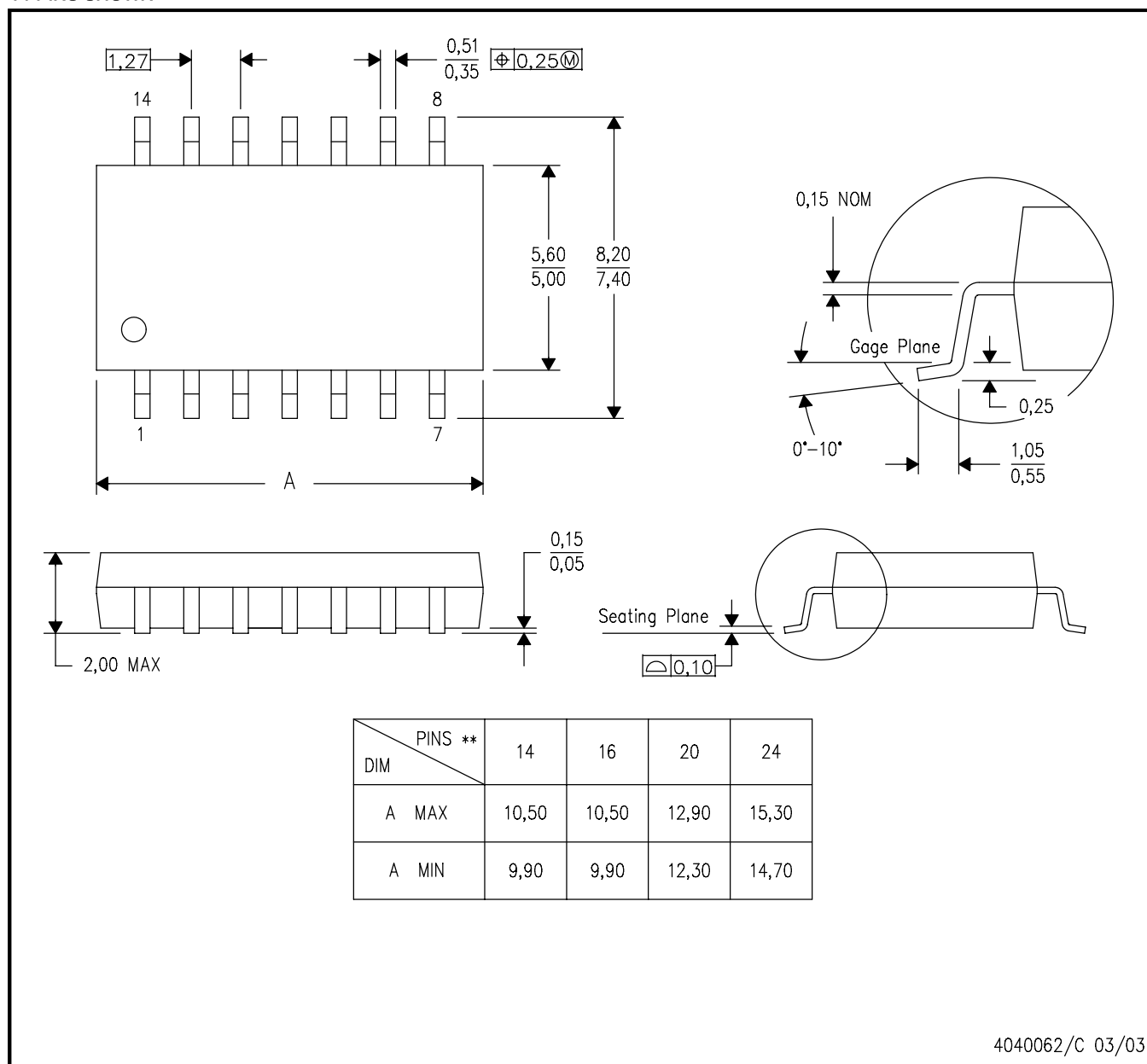


# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

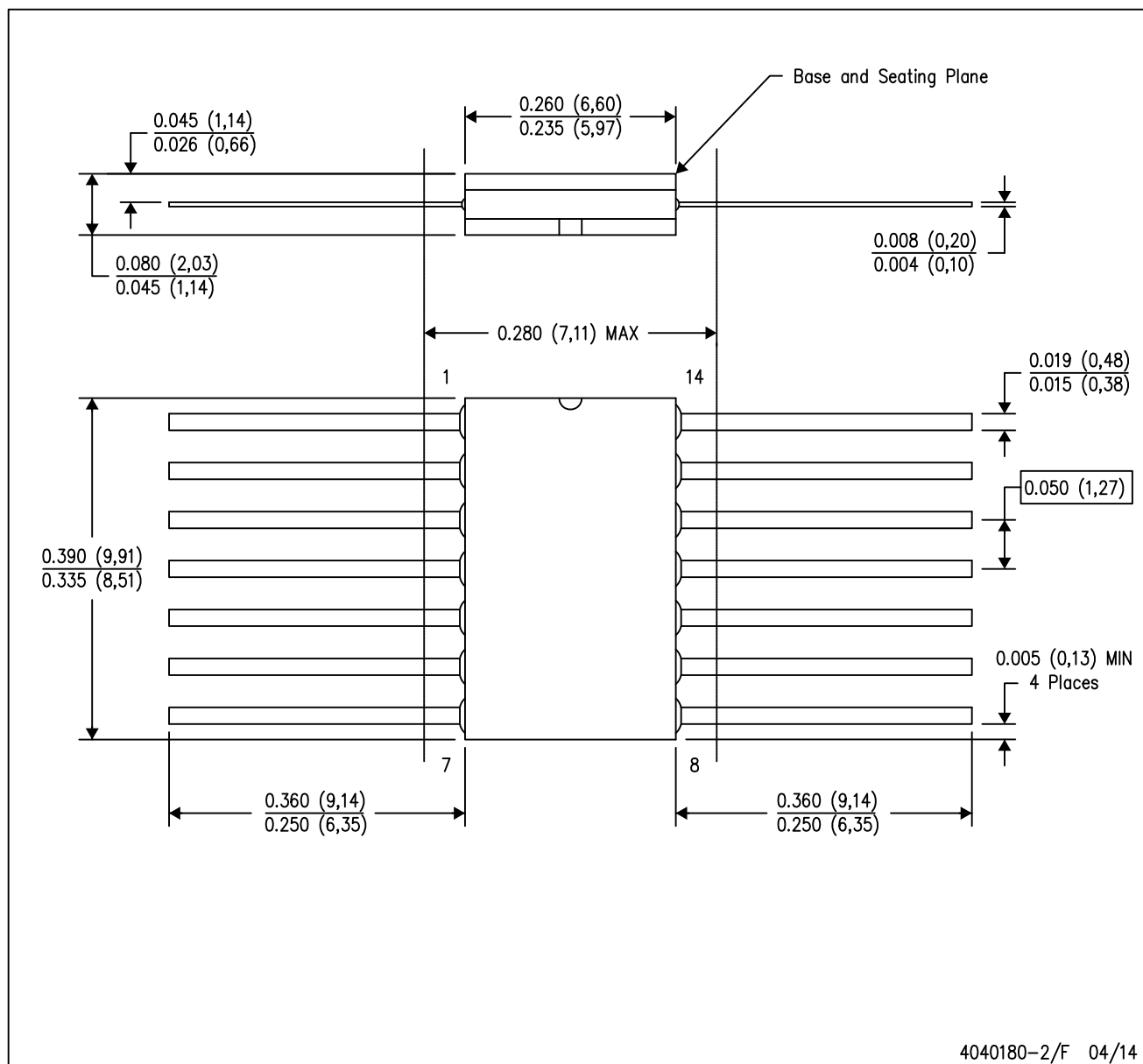


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

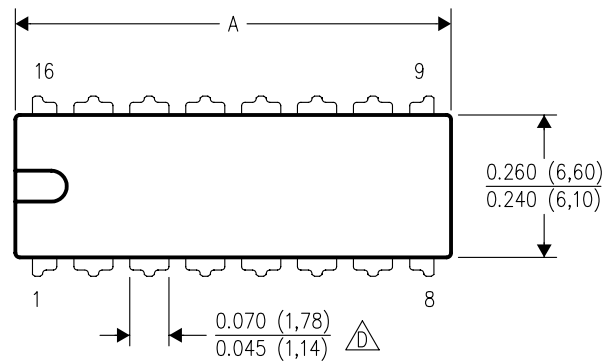
CERAMIC DUAL FLATPACK



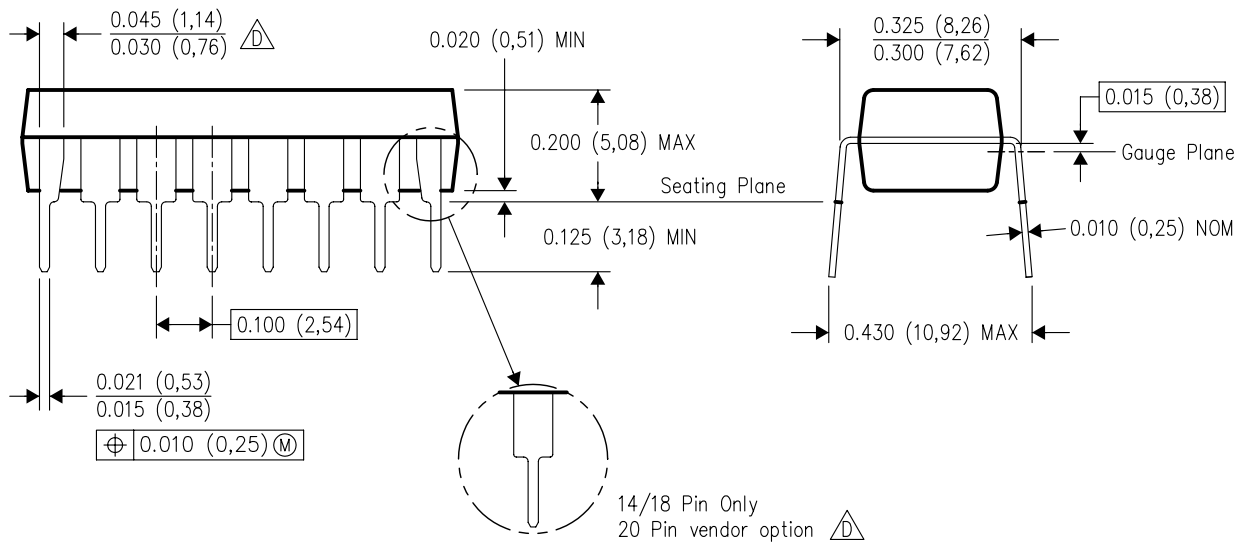
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

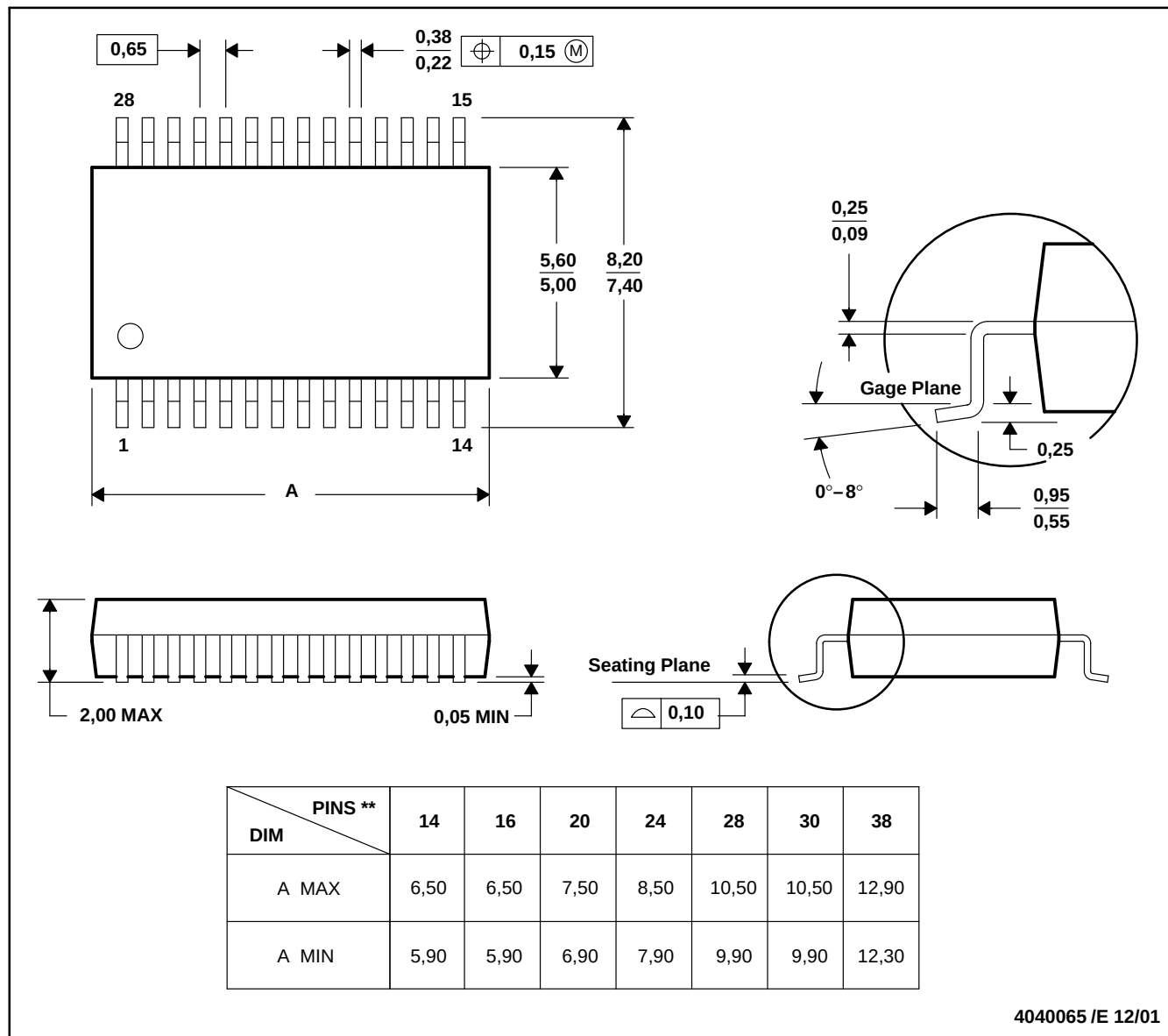
NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



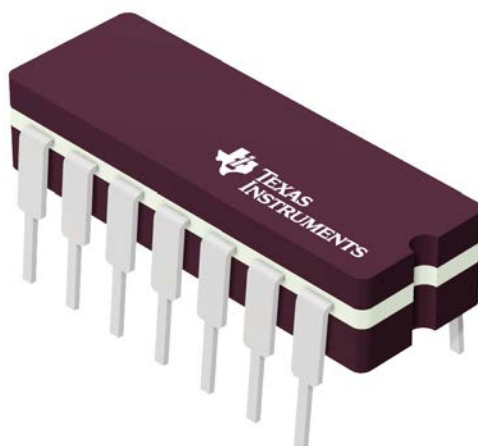
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

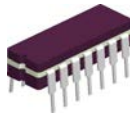
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

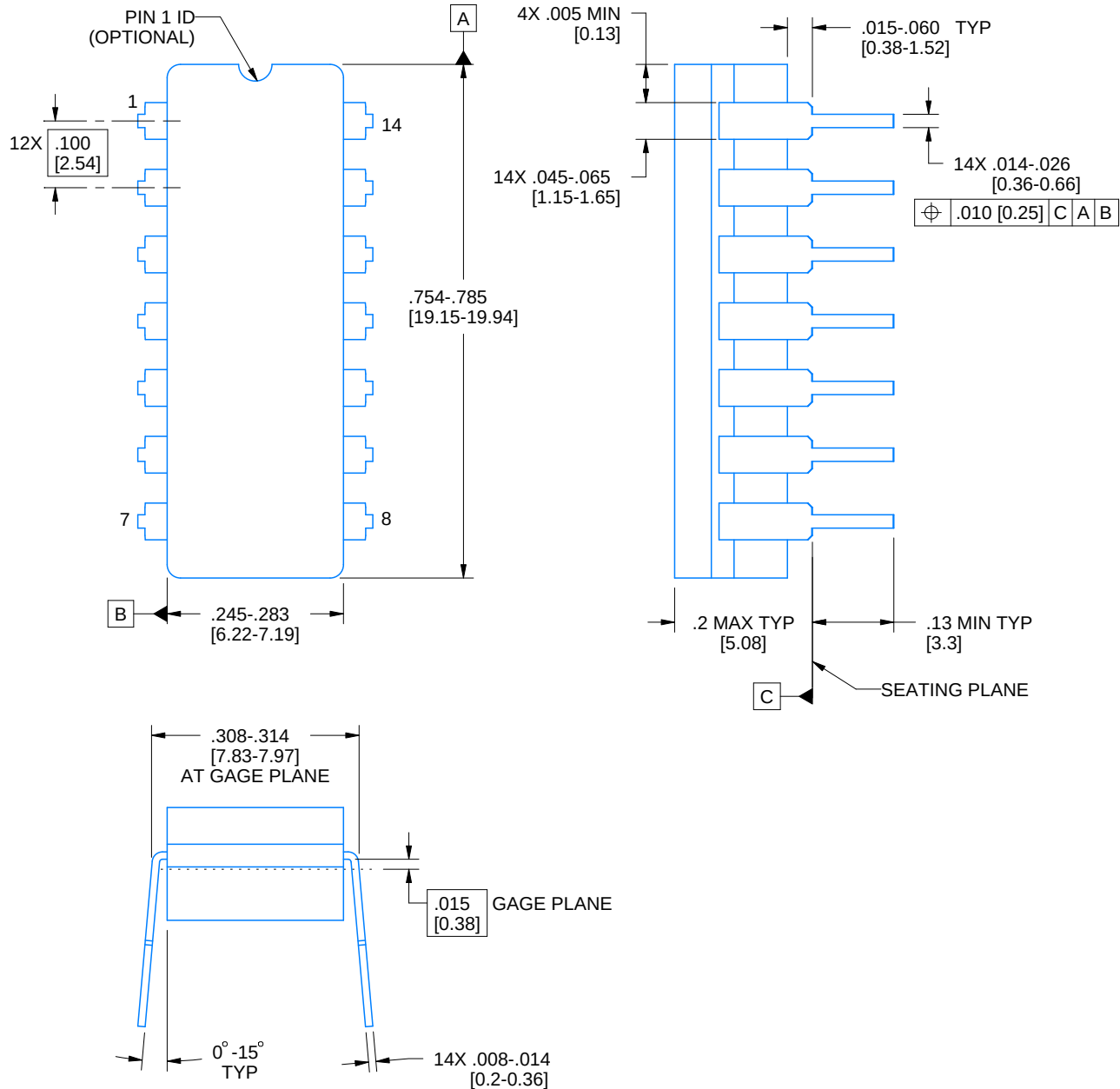
J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

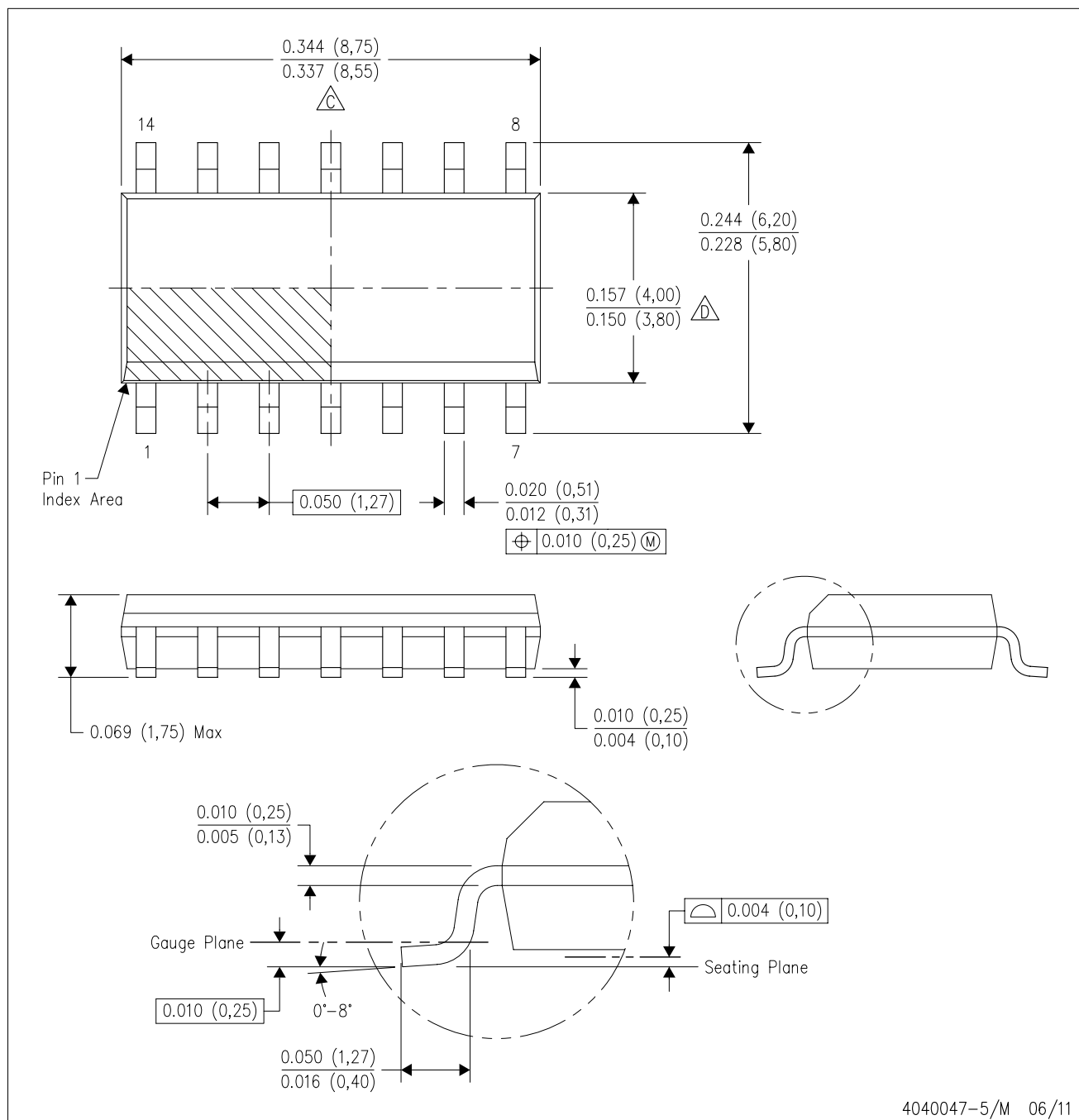
### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

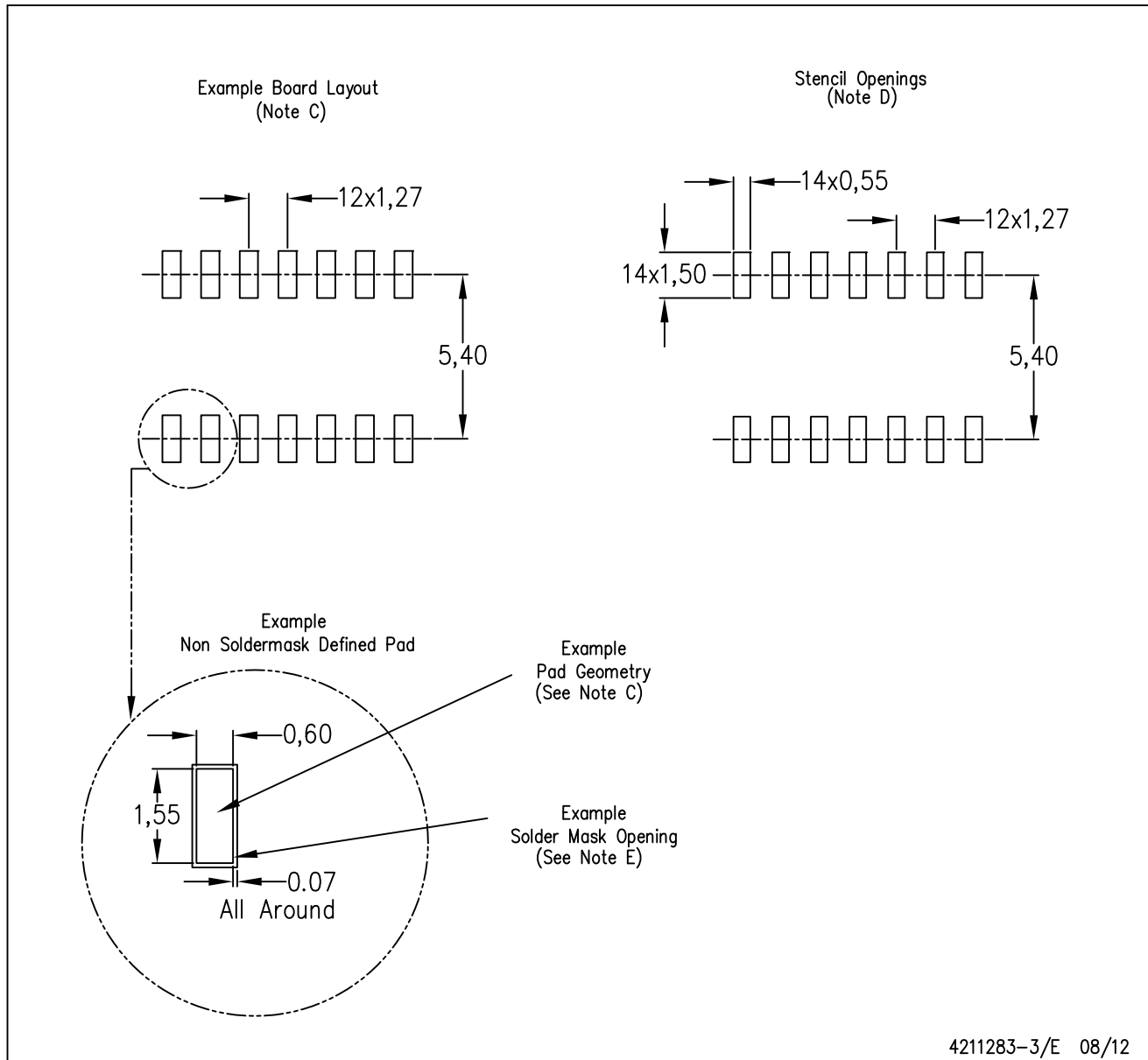


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

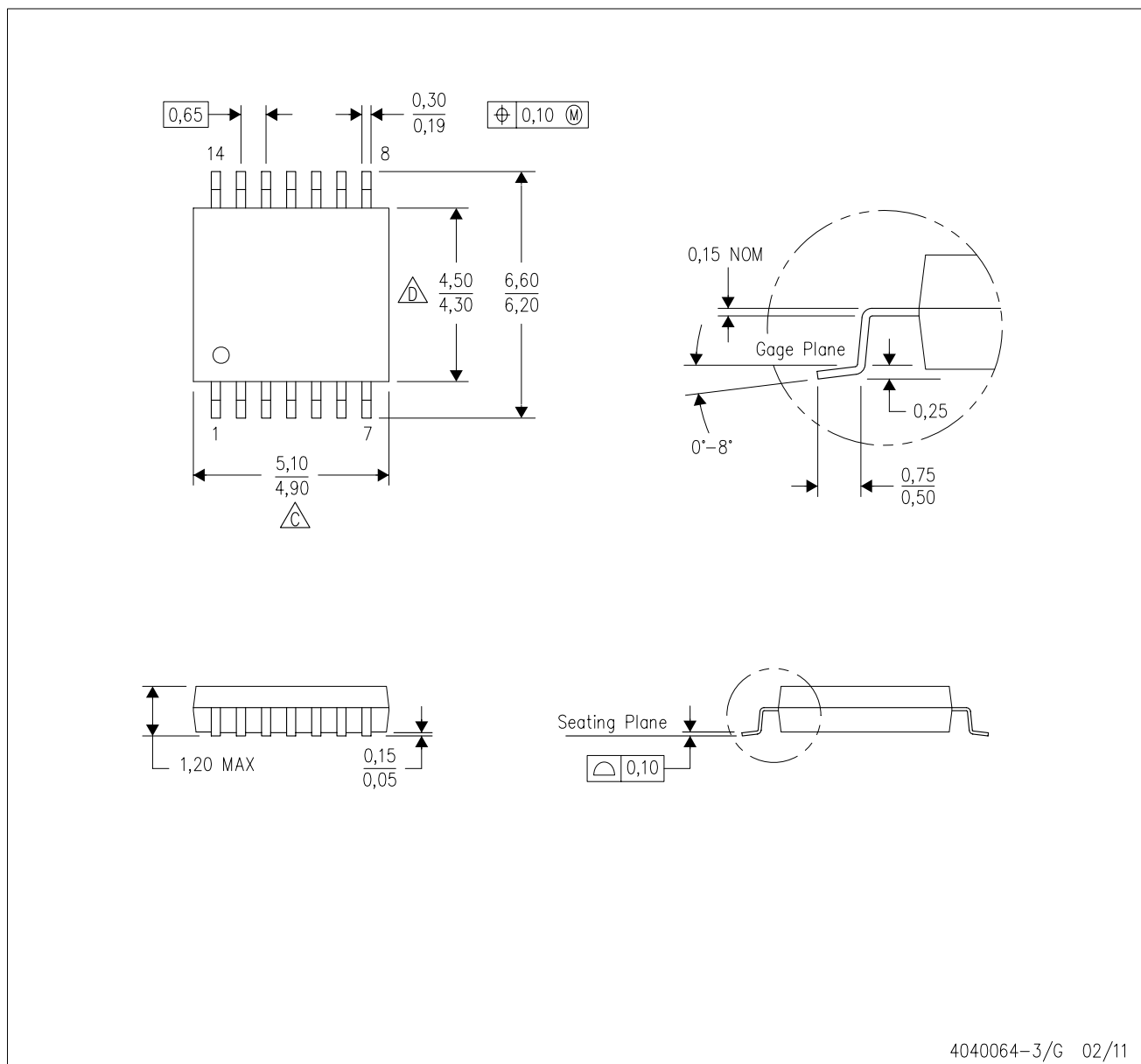


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

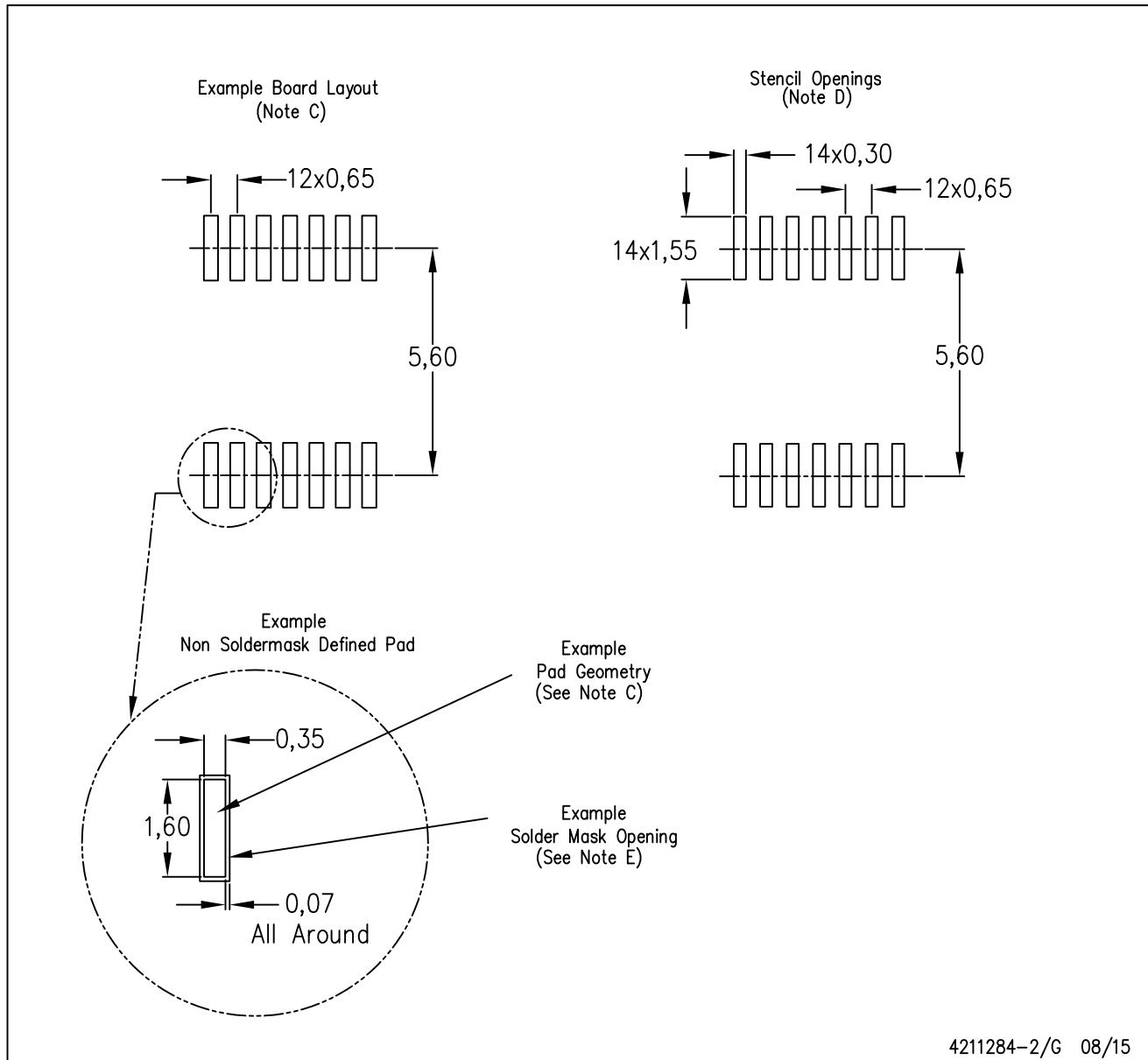
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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